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Shinya Tokunaga etal.
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For: Mask Pattern Checking Method, Checking Apparatus, Checking Data Used Therein and Checking Data Generating Method

STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir/Madam:

I, Satoshi Watanabe, of Ark Mori Building, 13F, 12-32, Akasaka 1-chome, Minato-ku, Tokyo 107-6028, Japan, hereby state that:

I well understand the Japanese and English languages and attached is an accurate English translation made by me of the Japanese specification in the above-identified U.S. patent application.

Date : February 1, 2006 Name : Satoshi W

Satoshi WATANABE

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[Inventor]
[Address] c/o Matsushita electric industrial co., ltd, 1006, Kadoma, Kadoma-shi, Osaka 571-8501 Japan
[Name] Shinya Tokunaga

[Inventor]
[Address] c/o Matsushita electric industrial co., ltd, 1006, Kadoma, Kadoma-shi, Osaka 571-8501 Japan
[Name] Hiroyuki Tsujikawa

[Inventor]
[Address] c/o Matsushita electric industrial co., ltd, 1006, Kadoma, Kadoma-shi, Osaka 571-8501 Japan
[Name] Tadashi Tanimoto

[Applicant for Patent]
[Identification Number] 000005821
[Appellation] Matsushita Electric Industry Co., Ltd.

[Agent]
[Identification No.] 100105647
[Attorney]
[Name or Appellation] Shohei Oguri
[Phone NO.] 03-5561-3990

[Selected Agent]

[Identification No.] 100105474
[Attorney]
[Name or Appellation] Hironori Honda
[Phone NO.] 03-5561-3990

[Selected Agent]
[Identification No.] 100108589
[Attorney]
[Name or Appellation] Toshimitsu Ichikawa
[Phone NO.] 03-5561-3990

[Selected Agent]
[Identification No.] 100115107
[Attorney]
[Name or Appellation] Takeshi Takamatsu
[Phone NO.] 03-5561-3990

[Selected Agent]
[Identification No.] 100090343
[Attorney]
[Name or Appellation] Yuriko Kuriu
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[Title of the Invention] Mask Pattern Checking Method, Checking Apparatus, Checking Data Used Therein and Checking Data Generating Method

[Claims]

[Claim 1] A method of checking a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising the steps of:

classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference and extracting the same;

determining checking precision for each of the ranks; and

deciding quality of the photomask depending on whether the determined checking precision is satisfied for each drawing pattern thus extracted.

[Claim 2] The method of checking a photomask according to claim 1, wherein the reference is a functional feature of the drawing pattern, and

the extracting step serves to classify the drawing pattern into a plurality of ranks and to extract the same depending on the functional feature of the drawing pattern.

[Claim 3] The method of checking a photomask according to claim 2, wherein the extracting step serves to classify the drawing pattern in the chip region of the semiconductor integrated circuit into a plurality of ranks and to extract the same depending on whether the drawing pattern is a dummy pattern.

[Claim 4] The method of checking a photomask according to claim 2, wherein the extracting step serves to classify the drawing pattern in the chip region of the semiconductor integrated circuit into a plurality of ranks and to extract the same depending on whether the drawing pattern has the same node.

[Claim 5] The method of checking a photomask according to any of claims 1 to 4, wherein the reference is a feature of a shape of the drawing pattern, and

the extracting step serves to classify the drawing pattern

into a plurality of ranks and to extract the same depending on the feature of the shape of the drawing pattern.

[Claim 6] The method of checking a photomask according to claim 5, wherein the extracting step serves to classify the drawing pattern into a plurality of ranks and to extract the same based on a distance from the closest pattern.

[Claim 7] The method of checking a photomask according to claim 5, wherein the extracting step serves to classify the drawing pattern into a plurality of ranks and to extract the same based on a distance from a corner of the drawing pattern.

[Claim 8] The method of checking a photomask according to any of claims 1 to 7, wherein the extracting step serves to classify the drawing pattern into the ranks and to extract the same depending on the reference for each pattern.

[Claim 9] The method of checking a photomask according to any of claims 1 to 7, wherein the extracting step serves to classify the drawing pattern into the ranks and to extract the same depending on the reference for each line (pattern edge).

[Claim 10] The method of checking a photomask according to any of claims 1 to 7, wherein the extracting step serves to classify the drawing pattern into the ranks and to extract the same depending on the reference for each area.

[Claim 11] The method of checking a photomask according to any of claims 1 to 9, wherein the deciding step serves to change a precision condition depending on an increase or decrease in a pattern width.

[Claim 12] The method of checking a photomask according to any of claims 1 to 11, wherein the deciding step serves to detect whether the drawing pattern is a dummy pattern and to relax the precision condition when the drawing pattern is the dummy pattern.

[Claim 13] The method of checking a photomask according to any of claims 1 to 12, wherein the deciding step serves to detect whether at least two patterns have the same node and to relax the precision condition when they have the same node.

[Claim 14] The method of checking a photomask according to any

of claims 1 to 12, wherein the deciding step serves to detect whether at least two patterns have the same node based on a pattern in the same layer and to relax the precision condition when they have the same node.

[Claim 15] The method of checking a photomask according to any of claims 1 to 12, wherein the deciding step serves to detect whether at least two patterns have the same node by a contact through a pattern in a layer positioned on or under the layer, and to relax the precision condition when they have the same node.

[Claim 16] The method of checking a photomask according to any of claims 1 to 12, wherein when the drawing pattern is a wiring pattern including a contact array,

the deciding step serves to detect whether one contact array or more is/are taken and to change the precision condition depending on whether one contact array or more is/are taken.

[Claim 17] The method of checking a photomask according to any of claims 1 to 12, wherein when the drawing pattern is a pattern for forming a contact hole,

the deciding step serves to detect whether one contact array or more is/are taken and to change the precision condition depending on whether one contact array or more is/are taken.

[Claim 18] The method of checking a photomask according to claim 1, wherein the extracting step serves to classify the drawing pattern into two ranks and to extract the same depending on whether a critical point determined by an intersection of a relational expression of a manufacturing defect density and a manufacturing defect size in a photomask and a relational expression of a pattern area weighed by a manufacturing defect generation probability on a pattern and the manufacturing defect size is exceeded based on the critical point.

[Claim 19] An apparatus for checking a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising:

means for classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks

in accordance with a predetermined reference and extracting a plurality of pattern data;

means for determining checking precision which is required for each of the ranks and generating precision data; and

means for deciding whether the pattern data satisfy the precision data for each of the classified pattern data.

[Claim 20] Checking data of a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising:

a plurality of pattern data extracted by a classification of a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference; and

precision data indicative of checking precision which is required for each of the ranks.

[Claim 21] A method of generating checking data of a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising the steps of:

classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference and extracting a plurality of pattern data; and

determining checking precision which is required for each of the ranks and generating precision data.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Belongs]

The present invention relates to a method of checking a mask pattern, a checking apparatus, checking data used therein and a method of generating the checking data, and more particularly to the extraction and check of checking precision data in a process for checking a photomask.

[0002]

[Prior Art]

In recent years, a semiconductor integrated circuit device (hereinafter referred to as an LSI) in each product is evaluated

as a key device, and an increase in the scale and speed of the LSI has been required in order to maintain the competitiveness of the product. A fine process is necessary with the microfabrication of an element and an increase in integration.

Under the circumstances, process conditions have been increasingly restricted in order to form a pattern as designed.

[0003]

In the formation of the semiconductor integrated circuit device, an isolation is carried out over the surface of a semiconductor substrate and a well having a desirable concentration is formed, and an impurity diffusion region having a desirable conductivity type is formed in the well, and furthermore, an insulating film is formed and a wiring pattern is provided.

[0004]

For example, in the formation of the wiring pattern, a photolithographic step of forming a conductive film such as a polycrystalline silicon layer, an aluminum layer or a metal silicide layer and then carrying out exposure through a photomask to form a desirable mask pattern is carried out, and etching is performed by using the mask pattern as a mask, thereby forming the wiring pattern.

[0005]

At the etching step, the conductive film exposed from the mask pattern is selectively removed. Even if various conditions such as the concentration and temperature of an etchant are optimized, an etching speed is varied depending on the density (area ratio) of the mask pattern, and furthermore, the peripheral length of the mask pattern. For this reason, precision in etching is varied depending on the density of the mask pattern or a pattern pitch. Even if a mask pattern region is excessively large or small, the precision in the etching is reduced.

[0006]

Moreover, the formation of a diffusion layer also has the same problems. If an ion implantation region for forming the diffusion layer is too small, the concentration of the ion is

generated so that a desirable diffusion profile cannot be obtained. Accordingly, the precision in the photomask for forming the mask pattern for diffusion is also very important.

[0007]

In each process, a pattern is formed by using the photomask. The pattern precision of the mask pattern on the photomask greatly depends on the precision in the pattern formation in the process. Therefore, a demand for an enhancement in the precision has been increased.

[0008]

Under the circumstances, at a defect checking step, necessary precision for a region which is to have the highest precision in a photomask to be checked is acquired from a photomask designer and a check is carried out by using a value thereof as a reference value. Thus, an effort to reduce the defect of the photomask has been made.

[0009]

For this reason, over one photomask, all regions are checked based on the same check reference. Therefore, a defect set within such a range as not to originally influence an actual circuit operation is treated to be present, and correction or manufacture is carried out again. Consequently, there is a problem in that a time (TAT) required from an order to a completion is increased.

Moreover, the photomask is expensive. Therefore, a sudden rise in a cost caused by the necessity of a large number of photomask blanks for carrying out the manufacture again is also a serious problem.

[0010]

In a recent process for manufacturing a semiconductor integrated circuit, moreover, there has been proposed a method of CMP (Chemical Mechanical Etching) for flattening the surface of a substrate. For example, this method serves to form an insulating film on a surface by a coating method of a CVD method and to then carry out chemical etching while performing mechanical polishing, thereby flattening the surface. In the

case in which the pattern density of a wiring layer to be a lower layer is low and there is a region including a pattern having a predetermined area or less, however, the flattening cannot be carried out even if the insulating film is formed thickly. As a result, a region having no wiring pattern after the CMP becomes a concave portion so that a dent state is maintained.

[0011]

In the case in which the layout pattern has a deviation, thus, sufficient pattern precision for the layer cannot be obtained. In addition, there is a problem in that the pattern precision of an upper layer is also influenced. Consequently, there is a problem in that the process precision cannot be sufficiently obtained.

[0012]

Therefore, the applicant has proposed a method of extracting the area ratio of the mask pattern from the layout pattern of a semiconductor chip, additionally providing a dummy pattern to the layout pattern to adapt the area ratio of the mask pattern of a layer constituting the layout pattern in consideration of the optimum area ratio of the layout pattern of the layer obtained based on the process conditions of the layer, thereby setting the layer to have the optimum area ratio (see Patent Document 1).

[0013]

[Patent Document 1]

JP-A-2002-229215

[0014]

A photomask to be a very important element in such an increase in precision in a pattern is used through a defect checking step.

Also in the check, necessary precision in a portion in which the toughest precision conditions in the photomask to be checked is acquired from the designer of the photomask and the check is carried out by using the data.

According to this method, it is possible to advance the check without specifying a place having the toughest portion

in the creation and check of the photomask. Thus, a yield can be enhanced.

[0015]

Description will be given to a conventional photomask checking flow with reference to the drawings.

Fig. 20 is a flow chart showing a conventional photomask check.

In this method, first of all, the pattern of a photomask is created based on a design rule (step 101). Next, the pattern of the photomask thus obtained is converted into data for photomask drawing and data are transferred to the manufacturing division of the photomask or another manufacturing company thereof so that a photomask is started to be actually manufactured (step 102).

[0016]

The minimum value of the design rule of a pattern is specified as check precision data when the data are thus transferred (step 106).

On the other hand, the photomask manufacturing division or another manufacturing company thereof draws a pattern on a photomask blank by using the drawing data of the photomask formed at the step 102, thereby forming the photomask (step 103).

Next, the result of the pattern formation is decided based on the checking precision data obtained at the step 106 (step 104).

Then, it is decided that only the pattern formation decided to be within the range of the checking precision data is acceptable.

[0017]

With the recent microfabrication of a process, however, a minimum pattern width and a minimum interval tend to be increasingly reduced. For example, consideration will be given to the case in which there is formed a photomask including patterns 210 to 213 having a minimum width which is arranged at a minimum interval 203 as shown in Fig. 21(a) and patterns 214 to 216 provided at a large interval 204 as shown in Fig. 21(b). For example,

it is assumed that the tolerance of a defect formed in a pattern having the minimum interval 203 is set to have a size represented by an allowable defect 201. At this time, in the case in which a pattern defect 206 having a smaller size than the size of the defect 201, it is decided that this is the tolerance at the checking step.

[0018]

In the case in which there is a pattern defect 202 having a greater size than the size of the allowable defect 201, moreover, it is decided that the photomask is a defect in the check because the defect 202 is larger than the allowable defect 201 at the checking step.

However, the allowable defect 201 has one size in the same photomask and the same processing is carried out based on the allowable defect 201 in any region having a great pattern width.

[0019]

[Problems that the Invention is to Solve]

For this reason, in the case in which there is the pattern defect 202 having a greater size than the size of the allowable defect 201, the interval 204 is much greater than the minimum interval 203 as shown in Fig. 21(b). Therefore, it is decided that the defect 202 is also a defect at the checking step between the patterns 214 and 215. Even if such a defect is thus present in the region having a great interval in an actual design rule, however, there is no problem. In spite of the foregoing, a correcting step is started so that a step of carrying out a check again is added.

[0020]

In the conventional method, thus, a demand for checking precision corresponding to the minimum interval 203 is given over the whole photomask. Therefore, it is decided that the defect 202 having such a size as not to make troubles is also a defect at the checking step.

[0021]

Also in the case in which the same defect is generated and patterns might be actually short-circuited with each other,

there is no problem when an adjacent pattern has the same node or a dummy pattern is formed for the purpose. Accordingly, it is not necessary to carry out the correction. However, the same defect is decided to be a defect in this case, the correcting step is started and the step of carrying out the check again is added.

Therefore, the check is executed with unnecessary precision so that a correction frequency is increased. Consequently, there is an obvious problem in that a reduction in a photomask creating period (TAT) and a decrease in the cost of creation are hindered.

[0022]

In consideration of the actual circumstances, the invention has been made and has an object to provide a method of checking a photomask which can shorten a TAT and decrease a cost.

It is another object to provide an apparatus for checking a photomask which can shorten the TAT and decrease the cost.

It is yet another object to provide checking data capable of shortening the TAT and decreasing the cost in order to create the photomask.

It is a further object to provide a method of generating checking data which can shorten the TAT and decrease the cost in order to create the photomask.

[0023]

[Means for Solving the Problems]

In order to attain the objects, a method according to the invention is characterized in that precision data on each pattern are extracted based on the feature of the pattern of a chip region and a check is carried out based on the precision data so that the check can be performed with high precision.

The chip region of a semiconductor integrated circuit indicates a functional region excluding the scribe line of a semiconductor chip.

[0024]

More specifically, the invention provides a method of

checking a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising the steps of classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference and extracting the same, determining checking precision for each of the ranks, and deciding quality of the photomask depending on whether the determined checking precision is satisfied. When a pad region has a large pattern, moreover, it is desirable that the pad region should be set to be a separate precision region having a low rank and the chip region excluding the pad region should be classified into a plurality of ranks to create checking data.
[0025]

According to this method, precision data on each pattern are extracted and are classified into a plurality of ranks to carry out the check with high precision based on the feature of the pattern of the chip region. Consequently, it is possible to create a photomask having a high reliability in a short time. Moreover, a sudden rise in a cost can be prevented from being caused by recreation to obtain unnecessary precision. Thus, the cost can be reduced.
[0026]

It is desirable that the check can be carried out more properly if the precision data are classified into a plurality of ranks and are thus extracted corresponding to the functional feature of the drawing pattern. The functional feature implies that the check is carried out in consideration of a feature based on the function of the pattern. For example, in the case in which the drawing pattern of the photomask includes the pattern of a gate electrode defining the channel length of a transistor or the case in which the drawing pattern of the photomask includes a mask pattern for ion implantation to form a pn junction to be a region defining a sensor area, these patterns are to have higher precision. In case of the same node or a dummy pattern, moreover, the precision may be lower than that in other regions. Thus, it is possible to classify the precision into ranks

corresponding to the functional feature of the pattern, thereby carrying out the check more properly at a high speed.

[0027]

It is desirable that the extracting step should serve to classify the drawing pattern in the chip region of the semiconductor integrated circuit into a plurality of ranks and to extract the same depending on whether the drawing pattern is a dummy pattern.

[0028]

It is desirable that the extracting step should serve to classify the drawing pattern in the chip region of the semiconductor integrated circuit into a plurality of ranks and to extract the same depending on whether the drawing pattern has the same node.

[0029]

It is desirable that the check can be carried out more properly if the drawing pattern is classified into a plurality of ranks and is thus extracted corresponding to the feature of the shape of the drawing pattern. For example, the check can be carried out more efficiently by a method of classifying the drawing pattern into a plurality of ranks and extracting the same based on a distance from the closest pattern, or classifying the drawing pattern into a plurality of ranks and extracting the same based on a distance from the corner of the drawing pattern.

[0030]

Moreover, the unit of the classification can easily be sliced by classifying each pattern into a plurality of ranks and extracting the same corresponding to the reference. Thus, the classification can efficiently be carried out.

[0031]

Referring to the unit of the classification, moreover, each line (pattern edge) is classified into a plurality of ranks and is thus extracted corresponding to the reference. In some cases, thus, small data are sufficient and an operation can easily be carried out. For example, in the case in which the classification is carried out depending on a distance from the

closest pattern, a data processing can easily be performed by using a check for each unit.

[0032]

Referring to the unit of the classification, furthermore, each area is classified into a plurality of ranks and is thus extracted corresponding to the reference. Consequently, slicing as a unit can be more simplified and the classification can efficiently be carried out. For example, in the case in which a plurality of patterns having the same node is extracted, the processing can easily be carried out by using a classifying method for each area.

[0033]

Desirably, a decision can be made more properly if the precision condition is changed to make the decision depending on an increase or decrease in the pattern width of the mask pattern of the photomask. For example, in case of a line and space pattern, it is necessary to use precision conditions considering a distance from the closest pattern to be set within a predetermined range or more when an error is made in such a direction as to increase the pattern width of the mask pattern. On the other hand, when the error is made in such a direction as to decrease the pattern width, it is necessary to use the precision conditions considering the pattern width to be a predetermined width or more.

[0034]

Whether the pattern is a dummy pattern is detected. If the precision conditions are relaxed when the pattern is the dummy pattern, it is possible to prevent a photomask to be originally acceptable from being rejected on unnecessary precision conditions.

[0035]

Moreover, whether a plurality of patterns has the same node is detected, and the precision conditions are relaxed when they have the same node. For example, if two adjacent patterns have the same node, they may be close to each other. If a contact is made through a plurality of contact holes, moreover, it is

preferable that any of contact hole patterns should function. In the case in which there is a plurality of patterns having the same node, thus, they may be conducted or any of them preferably functions in many cases and the precision conditions may be relaxed in many cases.

[0036]

In the case in which the same node is obtained by a pattern in the same layer, moreover, a decision can be made by only the drawing data. Consequently, a checking easiness is particularly high and this method is effective.

Also in the case in which a contact is made through a pattern in a layer positioned on the upper or lower layers so that the same node is obtained, furthermore, this method is effective.

[0037]

Moreover, when the drawing pattern is a wiring pattern including a contact array, the deciding step serves to detect whether one contact array or more is/are taken and to change the precision condition depending on whether one contact array or more is/are taken. In the case in which a plurality of contact arrays is taken, there is no problem of a characteristic if any of them is formed normally. Consequently, the precision condition may be relaxed.

[0038]

Furthermore, when the drawing pattern is a pattern for forming a contact hole, the deciding step serves to detect whether one contact array or more is/are taken and to change the precision condition depending on whether one contact array or more is/are taken. In the case in which a plurality of contact arrays is taken, similarly, there is no problem of a characteristic if any of them is formed normally. Consequently, the precision condition may be relaxed.

[0039]

A high-speed wiring region may be a high precision region.

Moreover, precision may be more decreased for an additional capacity region which is added in order to reduce a noise.

[0040]

It is desirable that the extracting step should serve to classify the drawing pattern into two ranks and to extract the same depending on whether a critical point determined by an intersection of a relational expression of a manufacturing defect density and a manufacturing defect size and a relational expression of a pattern area weighed by a manufacturing defect generation probability and the manufacturing defect size is exceeded based on the critical point. Consequently, it is possible to optimize the trade-off between a yield and a mask checking cost.

[0041]

It is desirable that an apparatus for checking a photomask for a semiconductor integrated circuit formed based on drawing pattern data should comprise means for classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference and extracting a plurality of pattern data, means for determining checking precision which is required for each of the ranks and generating precision data, and means for deciding whether the pattern data satisfy the precision data for each of the classified pattern data.

[0042]

Moreover, the invention provides checking data of a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising a plurality of pattern data extracted by a classification of the drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference, and precision data indicative of checking precision which is required for each of the ranks.

By using the data, it is possible to provide a photomask having a high reliability at a high speed with a low cost.

[0043]

The invention provides a method of generating checking data, comprising the steps of classifying a drawing pattern in a chip region of a semiconductor integrated circuit into a

plurality of ranks in accordance with a predetermined reference and extracting a plurality of pattern data, and determining checking precision which is required for each of the ranks and generating precision data.

According to the method, it is possible to form checking data capable of providing a photomask having a high reliability at a high speed with a low cost.

The chip region is a semiconductor region on a wafer and excludes a scribe line.

[0044]

[Mode for Carrying Out the Invention]

Next, description will be given to a photomask checking method according to an embodiment of the invention.

(First Embodiment)

In a photomask checking method according to the invention, when checking a photomask for a semiconductor integrated circuit formed based on drawing pattern data, a drawing pattern in a chip region of the semiconductor integrated circuit is classified into a plurality of ranks in accordance with a predetermined reference and is thus extracted, checking precision is determined for each of the ranks, and quality of the photomask is decided depending on whether the determined checking precision is satisfied.

[0045]

Fig. 1 shows a photomask checking flow according to the embodiment. While constant precision is specified from a design rule over a whole photomask in a conventional checking flow, checking precision data 306 are separately formed based on a photomask pattern obtained at a photomask pattern design step 101 and the check of the photomask is executed based on a checking precision reference set for each pattern area on the basis of the checking precision data 306.

[0046]

More specifically, first of all, the checking precision data 306 are separately formed based on the photomask pattern obtained at the photomask pattern design step 101.

[0047]

For example, as shown in a typical view of an example in Fig. 2, only a transistor region 2 is extracted from a layout pattern 1 of a polycrystalline silicon layer including a gate wiring. The transistor region 2 thus extracted is constituted by forming source and drain regions in an active region 4 surrounded by an isolating region (not shown) as shown in an enlarged view showing a main part in Fig. 3. A portion in which the gate wiring 3 is provided over the active region 4 acts as a portion for determining a channel length.

[0048]

As shown in Fig. 4, accordingly, a gate wiring 3T provided on the active region 4 is a region for greatly depending on a transistor characteristic. Therefore, pattern precision is to be very high. On the other hand, a region 3C other than the gate wiring 3T provided on the active region 4 may be rougher than the gate wiring 3T provided on the active region 4.

[0049]

In the pattern of the gate wiring 3, the gate wiring 3T provided on the active region 4 is set to be an A rank region RA and the gate wiring 3C, a gate other than the active region and whole other portions in the chip are set to be a B rank region RB, and these patterns are separately extracted. The pattern precision for the check is set to be higher in the A rank than that in the B rank and data are created in two stages.

[0050]

Thus, photomask drawing data (layout pattern data) are created at a step 102 based on the layout pattern data obtained at the photomask pattern design step 101.

Based on the layout pattern data obtained at the step 101, then, the pattern region is divided into two ranks having the A rank and the B rank and checking precision data 306 in each division are created.

[0051]

The checking precision data thus obtained are extracted together with the photomask drawing data obtained at the step

102 and are transferred to a photomask creating division or company.

[0052]

In the photomask creating division or company receiving the photomask drawing data obtained at the step 102 and the checking precision data 306 obtained at the step 306, thereafter, a pattern is continuously formed on a photomask blank through a photomask drawing process (step 103).

[0053]

Next, the defect of the photomask pattern thus formed is checked with necessary precision for each region based on the checking precision data 306 (step 104).

At the checking step 104, as shown in Fig. 5, only a region corresponding to the checking region having the A rank (RA in Fig. 4) is extracted from the formed photomask pattern (step 401) and it is decided whether the checking region is set within the range of the checking precision (step 402).

[0054]

If it is decided that the checking region is set within the range of the checking precision at the step 402, thereafter, it is decided whether the residual region, that is, the checking region having the B rank (a whole region other than RA in Fig. 4, that is, a region of a chip 1 in Fig. 2) is set within the range of the checking precision (step 403).

[0055]

If it is decided that the checking region is set within the range of the checking precision at the step 403, it is set to be acceptable and the processing proceeds to a shipping step 105 in Fig. 1.

On the other hand, if it is decided that the range of the checking precision is exceeded at the step 403, the checking region is set to be rejected and the processing returns to the step 103 again in which the photomask is manufactured.

If it is decided that the range of the checking precision is exceeded at the step 402, moreover, the checking region is set to be rejected and the processing returns to the step 103

again in which the photomask is manufactured.

[0056]

If the manufacture and the check are thus repeated and it is decided that there is no defect at the checking step 104, a check accepted product is shipped (step 105).

[0057]

According to this method, importance is particularly attached to the maintenance of a channel length to be the functional feature of a gate wiring, and a region to influence the channel length is set to be the region having the rank A and is caused to have higher pattern precision. In this method, accordingly, the check is carried out by using the checking precision data with high precision for only the region having the rank A requiring the high pattern precision, while a precision reference is more relaxed to carry out the check in the region having the rank B requiring no high pattern precision. Therefore, the check is not unnecessarily strict and the check is carried out in a short time, and furthermore, a checking defect is detected in an early stage. Correspondingly, a cost can be reduced.

[0058]

Thus, the check can be carried out with optimum checking precision in a short time and a photomask of high quality can be formed at a low cast. Moreover, a TAT can be shortened.

[0059]

At the deciding step, there is often employed a method of carrying out an observation based on the precision conditions while observing a pattern on the photomask by using a microscope. It is also possible to pick up an image by a CCD camera and to carry out an image processing using an image pick-up pattern as image data, thereby extracting a pattern and referring to precision data every extracted pattern to make a decision. For the decision itself, moreover, a comparative decision processing may be carried out by the image processing, thereby implementing an automatic processing.

[0060]

(Second Embodiment)

While the classification of the checking rank is specified for each region in the first embodiment, it may be specified for each pattern.

More specifically, as shown in Fig. 6, only the gate pattern of a region constituting a true gate region in the gate wiring 3 is set to be an A checking rank pattern PA corresponding to a checking rank with high precision, and the other patterns are set to be a B checking rank pattern PB corresponding to a lower rank.

[0061]

Also in this case, at a photomask checking step, the embodiment is the same as the first embodiment except that a method of extracting checking data and a checking reference are different.

By this method, similarly, a channel length can reliably be maintained and a photomask of high quality can be implemented in a short time at a low cost in the same manner as in the first embodiment. By this method, particularly, it is possible to produce an advantage that data indicative of a checking rank can be formed on drawing data (mask pattern data) as compared with the first embodiment.

[0062]

(Third Embodiment)

While the classification of the checking rank is specified for each region in the first embodiment, moreover, it may be specified by the edge of a pattern.

[0063]

More specifically, as shown in Fig. 7, only the gate pattern edge of a region constituting a true gate region in a gate wiring 3 is set to be an A checking rank edge EA corresponding to a checking rank with high precision, and the other patterns are set to be a B checking rank edge EB corresponding to a lower rank.

[0064]

Also in this case, the embodiment is the same as the first embodiment except that a method of extracting checking data and

a checking reference are different at a photomask checking step.

According to this method, it is possible to obtain an advantage that a deciding rank can be set every edge as compared with the first embodiment.

[0065]

(Fourth Embodiment)

Next, description will be given to a fourth embodiment of the invention.

While the checking method aiming at the maintenance of the channel length of a gate wiring in a transistor has been described in the first to third embodiments, description will be given to a checking method which particularly pays attention to the detection of a shift in the contact of a gate wiring pattern having a hole such as a contact hole and the prevention of a contact error in this example.

[0066]

Attention is paid to the presence of a contact hole h for a contact with the gate wiring of a transistor and a checking rank is classified.

More specifically, in the transistor array chip shown in Fig. 2, a region having the contact hole h over a gate wiring pattern 3 is particularly checked in a checking rank with high precision as shown in Fig. 8(a).

[0067]

As shown in Fig. 8(b), specification is carried out by a region, and a square region having a predetermined size which has a contact hole as a center is set to be an A checking rank region RA having a high precision rank and the other regions are set to be a B checking rank region RB, which are used as checking data.

At a checking step, the check is executed in accordance with the same flow chart as that shown in Fig. 5.

According to such a structure, the check is carried out with higher precision in the vicinity of the contact hole. Consequently, a contact error can be reduced and a photomask having a high reliability can be formed at a high speed.

[0068]

As a variant of the fourth embodiment, moreover, specification is carried out by a pattern, and only a gate pattern provided in the vicinity of the contact hole h in the gate wiring 3 is set to be an A checking rank pattern PA corresponding to a checking rank with high precision and the other patterns are set to be a B checking rank pattern PB corresponding to a lower rank as shown in Fig. 8(c).

[0069]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0070]

According to this method, it is possible to produce an advantage that a mask checking cost can be more reduced while suppressing a damage on a yield as compared with the first embodiment.

[0071]

As a variant of the fourth embodiment, moreover, specification is carried out by an edge, and only a gate pattern edge provided in the vicinity of the contact hole h in the gate wiring 3 is set to be an A checking rank edge EA corresponding to a checking rank with high precision and the other patterns are set to be a B checking rank edge EB corresponding to a lower rank as shown in Fig. 8(d).

[0072]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0073]

According to this method, it is possible to produce an advantage that a deciding rank can be set for each edge as compared with the first embodiment.

While the photomask for the gate wiring of a semiconductor integrated circuit constituting a transistor array has been described in the embodiment, it is apparent that the photomask

can also be applied to other semiconductor integrated circuits.
[0074]
(Fifth Embodiment)

Next, description will be given to a fifth embodiment of the invention.

In the first to third embodiments, there has been described the checking method which particularly attaches importance to the maintenance of the channel length to be the functional feature of the gate wiring of the transistor. In the fourth embodiment, there has been described the checking method which particularly attaches importance to the maintenance of the contact to be the functional feature of the gate wiring of the transistor. Both of these are functional features and description will be given to a checking method which particularly pays attention to the feature of a shape.
[0075]

Description will be given by taking, as an example, the photomask for a gate wiring to form the transistor array chip shown in Fig. 2.

In this example, a corner portion C of a pattern is slightly smooth except for a signal transmitting section of a high frequency circuit and does not influence a characteristic in many cases. Taking note of this respect, in the transistor array chip shown in Fig. 2, a region provided in the vicinity of the corner portion C is checked in a checking rank with particularly low precision over a gate wiring pattern 3 as shown in Fig. 9(a).
[0076]

As shown in Fig. 9(b), specification is carried out by a region determined through the wavelength of a light source for exposure and a pattern interval, and a square region is set to be a B checking rank region RB having a lower precision rank and the other regions are set to be an A checking rank region RA, which are used as checking data.

Referring to a checking step, a check is executed in accordance with the same flow chart as that shown in Fig. 5.
[0077]

First of all, the square region provided in the vicinity of the corner portion is set to be the B checking rank region RB having a lower precision rank and the other regions are set to be the A checking rank region RA as described above, and the defect of a photomask pattern which is formed is checked with necessary precision for each region based on checking precision data created with a classification into ranks in two stages (step 104).

[0078]

At the checking step 104, as shown in Fig. 10, only a region corresponding to a checking region having a B rank (see Fig. 9(b)) is extracted from the formed photomask pattern (step 1001), and it is decided whether the checking region is set within the range of the checking precision (step 1002).

[0079]

If it is decided that the checking region is set within the range of the checking precision at the step 1002, it is decided whether a residual region, that is, the checking region having the A rank (all regions other than B in Fig. 9(b)) is set within the range of the checking precision (step 1003).

If it is decided that the checking region is set within the range of the checking precision at the step 1003, a product is accepted and the processing proceeds to the shipping step 105 in Fig. 1.

[0080]

On the other hand, if it is decided that the checking region exceeds the range of the checking precision at the step 1003, the product is rejected and the processing returns to the step 103 again in which the photomask is manufactured.

[0081]

If it is decided that the checking region exceeds the range of the checking precision at the step 1002, moreover, the product is rejected and the processing returns to the step 103 again in which the photomask is manufactured.

[0082]

Thus, the manufacture and the check are repeated and a

product decided to have no defect at the checking step 104 is shipped as a checking accepted product (step 105).

[0083]

According to such a structure, attention is paid to the shape of a pattern and a region corresponding to the corner portion of the pattern is checked with precision reduced. Therefore, a variation which does not make troubles of functions is set to be acceptable. Thus, a product which is originally decided to be rejected by the check is accepted. Thus, a yield can be enhanced and a photomask having a high reliability can be formed at a high speed.

[0084]

As a variant of the fifth embodiment, moreover, specification is carried out by a pattern, and only a pattern in the corner of the gate wiring 3 is set to be a B checking rank pattern PB corresponding to a checking rank with low precision and the other patterns are set to be an A checking rank pattern PA corresponding to a higher rank as shown in Fig. 9(c). Herein, the rank is determined based on a distance from the corner.

[0085]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0086]

By this method, similarly, it is possible to produce an advantage that data indicative of the checking rank can be particularly formed on drawing data (mask pattern data) as compared with the first embodiment.

[0087]

As a variant of the fifth embodiment, moreover, specification is carried out by an edge, and only a pattern edge in the corner portion of the gate wiring 3 is set to be a B checking rank edge EB corresponding to a checking rank with low precision and the other patterns are set to be an A checking rank edge EA corresponding to a higher rank as shown in Fig. 9(d).

[0088]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0089]

According to this method, it is possible to produce an advantage that a deciding rank can be set for each edge as compared with the first embodiment.

[0090]

While the photomask for the gate wiring of a semiconductor integrated circuit constituting a transistor array has been described in the embodiment, it is apparent that the photomask can also be applied to other semiconductor integrated circuits.

[0091]

(Sixth Embodiment)

Next, a sixth embodiment of the invention will be described.

In the invention, description will be given to a checking method in which a classification is carried out based on the feature of a shape, particularly, the interval of a wiring, thereby dividing a precision rank successively to the fifth embodiment.

[0092]

Description will be given by taking, as an example, the photomask for a gate wiring to form the transistor array chip shown in Fig. 2.

In this example, the photomask is applied to the case in which the formation is carried out through a process for generating a defect in such a direction that the pattern is thickened, and the checking standards of a region having a small line width in a region in which a wiring is particularly formed on the pattern at a high density are set to be high and the checking standards of the other regions are set to be low. In the transistor array chip shown in Fig. 2, lines 11a, 11b and 11c are arranged in a line and space region as shown in Fig. 11(a). Taking note of intervals w1 and w2 between these lines, a region

in which the interval w1 has a certain value or less is set to be a higher checking region, and the other regions are particularly checked in a checking rank having precision reduced.
[0093]

As shown in Fig. 11(b), specification is carried out by a region, and a region having a small line interval w1 is set to be an A checking rank region RA having a higher precision rank and the other regions are set to be a B checking rank region RB, which are used as checking data.

At a checking step, the check is executed in accordance with the same flow chart as that shown in Fig. 5.
[0094]

Thus, the manufacture and the check are repeated and a product decided to have no defect at the checking step 104 is shipped as a checking accepted product (step 105).
[0095]

According to such a structure, attention is paid to the shape of a pattern and a region having a small line interval is checked with an increase in precision. Therefore, the check is carried out with high precision for only a region requiring a high precision pattern. Consequently, a product which is originally decided to be rejected by the check is accepted. Thus, a yield can be enhanced and a photomask having a high reliability can be formed at a high speed.
[0096]

As a variant of the sixth embodiment, moreover, specification is carried out by a pattern, and only a pattern having a small line interval in a gate wiring 3 is set to be an A checking rank pattern PA corresponding to a checking rank with high precision and the other patterns are set to be a B checking rank pattern PB corresponding to a lower rank as shown in Fig. 11(c).
[0097]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0098]

According to this method, similarly, it is possible to produce an advantage that data indicative of the checking rank can be particularly formed on drawing data (mask pattern data) as compared with the first embodiment.

[0099]

As a variant of the sixth embodiment, moreover, specification is carried out by an edge, and only a pattern edge of a pattern having a small wiring interval in the gate wiring 3 is set to be an A checking rank edge EA corresponding to a checking rank with high precision and the other patterns are set to be a B checking rank edge EB corresponding to a lower rank as shown in Fig. 11(d).

[0100]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0101]

According to this method, it is possible to produce an advantage that a deciding rank can be set for each edge as compared with the first embodiment.

[0102]

While the photomask for the gate wiring of a semiconductor integrated circuit constituting a transistor array has been described in the embodiment, it is apparent that the photomask can also be applied to other semiconductor integrated circuits.

[0103]

(Seventh Embodiment)

Next, a seventh embodiment of the invention will be described.

In the embodiment, description will be given to a checking method in which a classification is carried out based on the feature of a shape, particularly, a wiring width, thereby dividing a precision rank successively to the sixth embodiment.

[0104]

Description will be given by taking, as an example, the

photomask for a gate wiring to form the transistor array chip shown in Fig. 2.

In this example, the photomask is applied to the case in which the formation is carried out through a process for generating a defect in such a direction that the pattern is thinned, and the checking standards of a region having a small line width in a region in which a wiring is particularly formed on the pattern at a high density are set to be high and the checking standards of the other regions are set to be low, which are used as checking data. In the transistor array chip shown in Fig. 2, lines 12a and 12b are arranged in a line and space region as shown in Fig. 12(a). Taking note of line widths L1 and L2, a region in which the line width L1 has a predetermined value or less is set to be a higher checking region, and the other regions are particularly checked in a checking rank having precision reduced.
[0105]

As shown in Fig. 12(b), specification is carried out by a region, and a region having a small line width L1 is set to be an A checking rank region RA having a higher precision rank and the other regions are set to be a B checking rank region RB.

At a checking step, the check is executed in accordance with the same flow chart as that shown in Fig. 5.
[0106]

Thus, the manufacture and the check are repeated and a product decided to have no defect at the checking step 104 is shipped as a checking accepted product (step 105).
[0107]

According to such a structure, attention is paid to the shape of a pattern and a region having a small line width is checked with an increase in precision. Therefore, the check is carried out with high precision for only a region requiring a high precision pattern. Consequently, a product which is originally decided to be rejected by the check is accepted. Thus, a yield can be enhanced and a photomask having a high reliability can be formed at a high speed.

[0108]

As a variant of the seventh embodiment, moreover, specification is carried out by a pattern, and only a pattern having a small line width in a gate wiring 3 is set to be an A checking rank pattern PA corresponding to a checking rank with high precision and the other patterns are set to be a B checking rank region PB corresponding to a lower rank as shown in Fig. 12(c).

[0109]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0110]

According to this method, similarly, it is possible to produce an advantage that data indicative of the checking rank can be particularly formed on drawing data (mask pattern data) as compared with the first embodiment.

[0111]

As a variant of the sixth embodiment, moreover, specification is carried out by an edge, and only a pattern edge of a pattern having a small wiring width in the gate wiring 3 is set to be an A checking rank edge EA corresponding to a checking rank with high precision and the other patterns are set to be a B checking rank edge EB corresponding to a lower rank as shown in Fig. 12(d).

[0112]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0113]

According to this method, as compared with the embodiments, it is possible to produce an advantage that a yield can be maintained stably without depending on the direction of a defect (an increase and decrease in the pattern width) as compared with the embodiments.

[0114]

While the photomask for the gate wiring of a semiconductor integrated circuit constituting a transistor array has been described in the embodiment, it is apparent that the photomask can also be applied to other semiconductor integrated circuits.

[0115]

(Eighth Embodiment)

Next, an eighth embodiment of the invention will be described.

In the embodiment, description will be given to a method of checking a photomask for forming a contact hole and checking data. Description will be given to a checking method of carrying out a classification and dividing a precision rank to relax checking standards in the case in which a functional feature, that is, a plurality of contact holes having the same node is present successively to the first embodiment.

[0116]

Description will be given by taking, as an example, a photomask for forming a contact hole which serves to form the transistor array chip shown in Fig. 2.

This example is applied to the case in which a defect is generated in such a direction that a pattern is thinned, that is, the case in which an etching section is tapered by isotropic etching. Therefore, checking standards in a region on a pattern where a plurality of contact holes having the same node is present are set to be lower than those in the other regions. In the transistor array chip shown in Fig. 2, when contact hole patterns 13a and 13b shown in Fig. 13(a) are arranged, attention is paid to these forming situations and the region where a plurality of contact holes having the same node is present is particularly checked in a checking rank with lower precision than that in the other regions.

[0117]

As shown in Fig. 13(b), specification is carried out by a region, and a region in which a plurality of contact holes having the same node is present is set to be a B checking rank region RB having a lower precision rank and the other regions

are set to be an A checking rank region RA, which are used as checking data.

At a checking step, the check is executed in accordance with the same flow chart as that shown in Fig. 10.

[0118]

Thus, the manufacture and the check are repeated and a product decided to have no defect at the checking step 104 is shipped as a checking accepted product (step 105).

[0119]

According to such a structure, attention is paid to the shape situation of a pattern and a region in which a plurality of contact holes having the same node is present is checked in a lower precision rank. Therefore, a product which is originally decided to be rejected by the check is accepted. Thus, a yield can be enhanced and a photomask having a high reliability can be formed at a high speed.

[0120]

As a variant of the eighth embodiment, moreover, specification is carried out by a pattern, and only a pattern 13b in which a plurality of contact holes having the same node is present is set to be a B checking rank pattern PB corresponding to a checking rank with low precision and the other regions are set to be an A checking rank pattern PA corresponding to a higher rank as shown in Fig. 13(c).

[0121]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0122]

According to this method, it is possible to produce an advantage that data indicative of the checking rank can be formed on drawing data (mask pattern data).

[0123]

As a variant of the eighth embodiment, moreover, specification is carried out by an edge, and a pattern edge of a contact hole edge where a plurality of contact holes having

the same node is present is set to be a B checking rank edge EB corresponding to a checking rank with lower precision and the other regions are set to be an A checking rank edge EA corresponding to a higher rank as shown in Fig. 13(d).

[0124]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0125]

According to this method, it is possible to produce an advantage that a deciding rank can be set for each edge as compared with the first embodiment.

[0126]

While the photomask for the gate wiring of a semiconductor integrated circuit constituting a transistor array has been described in the embodiment, it is apparent that the photomask can also be applied to other semiconductor integrated circuits.

[0127]

Moreover, the case in which a plurality of contact holes having the same node is present in a close region has been described in the embodiment. From a viewpoint in which it is sufficient that a contact can be made through any contact hole, it is preferable that the same checking method should be used also when the contact holes having the same node are present in separated positions.

[0128]

While the description will be given to the check to be carried out in such a direction that the pattern is thinned in the process, that is, the size of the contact hole is decreased in the embodiments, moreover, the same check is carried out for etching in such a direction that overetching is generated to thicken the pattern, that is, the size of an opening region is increased.

[0129]

(Ninth Embodiment)

Next, a ninth embodiment of the invention will be

described.

In the eighth embodiment, the description has been given to the method of checking a photomask for forming a contact hole and the checking data. In this example, description will be given to a checking method of carrying out a classification to divide a precision rank in order to relax checking standards when a defect is generated in such a direction that a pattern is thickened in case of a functional feature, particularly, a pattern having the same node successively to the eighth embodiment in a photomask for forming a wiring pattern such as a gate wiring.

[0130]

Description will be given by taking, as an example, the photomask for forming a contact hole which serves to form the transistor array chip shown in Fig. 2.

This example is applied to the case in which a defect is generated in such a direction that a pattern is thickened, and checking standards in a region including the patterns having different nodes in a region are set to be higher than the checking standards of the other regions. In the transistor array chip shown in Fig. 2, when lines 14a and 14b shown in Fig. 14(a) are arranged, attention is paid to these functional situations and a region including the patterns having different nodes is checked in a checking rank with particularly higher precision than that in the other regions.

[0131]

As shown in Fig. 14(b), specification is carried out by a region, and a region in which a plurality of patterns having different nodes is present is set to be an A checking rank region RA and the region having the same node is set to be a B checking rank region RB. The precision is reduced to more decrease the checking rank of precision in the B checking rank region than that in the A checking rank region RA and this is used as checking data.

At a checking step, the check is executed in accordance with the same flow chart as that shown in Fig. 10.

[0132]

Thus, the manufacture and the check are repeated and a product decided to have no defect at the checking step 104 is shipped as a checking accepted product (step 105).

[0133]

According to such a structure, attention is paid to the shape situation of a pattern, and only a region in which the patterns having the different nodes is checked in a higher precision rank and a region in which a plurality of patterns having the same node is present is checked in a lower precision rank. Therefore, a product which is originally decided to be rejected by the check is accepted. Thus, a yield can be enhanced and a photomask having a high reliability can be formed at a high speed.

[0134]

As a variant of the ninth embodiment, moreover, specification is carried out by a pattern, and only the pattern 14b in which a plurality of patterns having different nodes is present is set to be an A checking rank pattern PA corresponding to a checking rank with high precision and the other regions are set to be a B checking rank pattern PB corresponding to a lower rank as shown in Fig. 14(c).

[0135]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0136]

According to this method, it is possible to produce an advantage that data indicative of the checking rank can be formed on drawing data (mask pattern data).

[0137]

As a variant of the ninth embodiment, moreover, specification is carried out by an edge, and an adjacent pattern edge of the pattern edge having the same node is set to be a B checking rank edge EB corresponding to a checking rank with lower precision and the other patterns are set to be an A checking

rank edge EA corresponding to a higher rank as shown in Fig. 14(d).

[0138]

Also in this case, the same photomask checking step as that in the embodiments is executed except that a method of extracting checking data and a checking reference are different.

[0139]

According to this method, it is possible to produce an advantage that a deciding rank can be set for each edge as compared with the first embodiment.

[0140]

While the photomask for the gate wiring of a semiconductor integrated circuit constituting a transistor array has been described in the embodiment, it is apparent that the photomask can also be applied to other semiconductor integrated circuits.

In the embodiments, furthermore, it is decided whether the same node is used depending on whether the patterns in the same layer are connected to each other. By carrying out a connection through a contact hole over the upper or lower layer, it is also possible to carry out a classification based on the same node also in the case in which the same node is to be constituted.

[0141]

(Tenth Embodiment)

Next, a tenth embodiment of the invention will be described.

While the checking data are formed based on the layout pattern of a semiconductor integrated circuit in the embodiments, information taking note of a circuit function may be extracted from a net list to classify a checking rank. Fig. 15 is a flow chart.

[0142]

More specifically, a critical net is extracted from a net list (step 1501).

The critical net includes a clock net, a timing constraint setting net, an analog net and a high-speed signal net.

A layout pattern is extracted from the critical net (step 1502).

Pattern data for a photomask are extracted from the layout pattern (step 1503).

Then, a checking rank is classified corresponding to each function (step 1504).

Thus, information is extracted from the net list based on a classification reference to which attention is paid. Consequently, it is possible to extract checking data at a higher speed.

[0143]

(Eleventh Embodiment)

Next, an eleventh embodiment of the invention will be described.

While the description has been given to the checking method of forming checking data and using the same in the embodiments, a method of determining the threshold of checking precision will be described in the embodiment.

The embodiment is characterized in that the threshold of the checking precision is determined based on a critical point determined by an intersection of a relational expression of the sum of pattern areas weighed at the manufacturing defect generation probability of a photomask for a semiconductor integrated circuit and a manufacturing defect size and a relational expression of a manufacturing defect density and the manufacturing defect size.

[0144]

In this example, as shown in Fig. 16, there is obtained an intersection C of a relational curve A of the sum of the pattern areas weighed at the manufacturing defect generation probability of the photomask and the manufacturing defect size and a relational curve De(x) of the manufacturing defect density and the manufacturing defect size. A check with higher precision is used for a smaller pattern than C.

The reason is as follows. A yield is calculated from an area RD to be a product of the relational curve A and the relational

curve De(x). In a smaller region than the intersection C, a fluctuation in a pattern dimension directly influences the yield.

Herein, an axis of ordinate indicates the sum of the pattern areas weighed at the manufacturing defect generation probability and the manufacturing defect density, and an axis of abscissa indicates the manufacturing defect size.

[0145]

The threshold of the weighing of the manufacturing defect generation probability to be used in the relational curve A is determined based on a method shown in Figs. 17(a) to 17(c).

This method investigates the case in which defects D1 to D3 are formed on a pattern on the assumption of a line and space Ln having a line width of l and an interval of S.

As shown in Fig. 17(a), when a size x of the defect D1 is smaller than the interval S, there is no short-circuit defect.

As shown in Fig. 17(b), moreover, when the size x of the defect D1 is greater than the interval S and is smaller than 21+S, there is a short-circuit defect according to circumstances.

As shown in Fig. 17(c), furthermore, when the size x of the defect D1 is greater than 21+S, there is the short-circuit defect.

In the case in which an open defect is generated, moreover, the open defect and an interval between a line and a space are reversed to each other.

[0146]

(Twelfth Embodiment)

Next, a twelfth embodiment of the invention will be described.

In the embodiment, a structure is formed in order to optimize an area ratio in a manufacturing process and to reduce a noise through an additional capacity in a semiconductor integrated circuit chip. With this structure, a bypass capacitor having an MOS structure using a diffusion region of the same conductivity type as that of a substrate (P well) is automatically provided as a bypass capacitor under a power wiring region extended to an empty region, and a substrate contact

provided under a ground wiring and the bypass capacitor provided under the power wiring are coupled to each other through a diffusion. Description will be given to a method of checking a photomask for forming the structure.

[0147]

More specifically, Figs. 18(a) to (c) (Figs. 18(b) and (c) are A-A and B-B sectional views of Fig. 18(a), respectively) are views showing a semiconductor integrated circuit formed by using a photomask obtained by the checking method according to the embodiment. Fig. 18(a) is a plan view in which the substrate contact is provided under the ground wiring and a bypass capacitor having an MOS structure using a diffusion region of the same conductivity type as that of a substrate is automatically provided as a bypass capacitor under a power wiring, and the substrate contact provided under the ground wiring and the bypass capacitor provided under the power wiring are coupled to each other through a diffusion.

[0148]

According to the embodiment, the bypass capacitor is automatically provided under the power wiring extended to the empty region so that the area ratio in the manufacturing process can be optimized, and furthermore, the pattern of a ground wiring 1805 and a substrate contact formation diffusion region 1816 do not need to have high precision in the region extended to the empty region when the area of the chip is increased. Moreover, the substrate contact formation diffusion region 1816 formed under the ground wiring 1805 is extended and connected to a bypass capacitor formation diffusion region 1815 provided under a power wiring 1801. Consequently, the power wiring and the bypass capacitor, and the ground wiring 1805 and the bypass capacitor are connected to each other through a lower resistance than that of the substrate having a high resistance. Also in this functional sense and because of a large number of contacts 1807 provided in the same node, high precision is not required.

Accordingly, a pattern region for forming an additional capacity which is provided in the empty region is a dummy pattern

having the same node, and a pattern region having lower precision is set to be a B rank region RB and a pattern region for forming the other regions is set to be an A rank region RA requiring the conditions with higher precision. Consequently, it is possible to obtain a photomask having a high reliability at a high speed and a low cost.

[0149]

Figs. 18(a) to 18(c) are plan views showing a graphic pattern according to the embodiment of the invention, in which a substrate contact is provided under the ground wiring 1805 and a bypass capacitor having an MOS structure using a diffusion region of the same conductivity type as that of the substrate is automatically provided as a bypass capacitor under the power wiring 1 extended to an additional formation region, and a substrate contact provided under the ground wiring and the bypass capacitor provided under the power wiring are coupled to each other through a diffusion. A diffusion region 1817 for forming the bypass capacitor and the diffusion region 1816 for the substrate contact have the same polarity and are formed integrally with each other.

[0150]

(Thirteenth Embodiment)

Next, a thirteenth embodiment of the invention will be described.

As shown in Fig. 14(c) in the ninth embodiment, furthermore, the description has been given to the classification of the line pattern 14b having the rank A and the line pattern 14a having the rank B in the line and space pattern. There will be considered an example of a classification in which a dummy pattern 14c is formed between the line pattern 14b having the rank A and the line pattern 14a having the rank B.

[0151]

In the embodiment, a classification into pattern ranks PA and PB is carried out, and furthermore, the dummy pattern is set to be a pattern rank PC which may have lower precision and checking precision is reduced.

Consequently, a yield can be enhanced and a photomask having a high reliability can be formed at a higher speed.

If the classification is carried out in two stages, that is, the precision rank is once classified depending on whether a pattern has the same node, and furthermore, whether the pattern is dummy, thus, the processing can be carried out at a higher speed so that the yield can be enhanced.

Moreover, a classification in a plurality of stages is also effective, that is, the classification is carried out based on the feature of a shape and is further performed based on a functional feature.

[0152]

(Fifteenth Embodiment)

Next, a fifteenth embodiment of the invention will be described.

While only the mask pattern to be resolved over the wafer has been described in the embodiments, it is necessary to change checking precision for the mask pattern which is not resolved over the wafer. In some cases, furthermore, it is necessary to consider the relationship between the function of the mask pattern itself and a peripheral pattern.

In the embodiment, description will be given to the check of a mask using a mask technique in which a density is substantially made uniform by the addition of very small graphics.

As shown in Fig. 21, a so-called assist bar (a scattering bar) uses a body pattern 601 to be body data, and four assist bars 602a to 602d separated from the body pattern 601 along the peripheral edge of the body pattern 601 by a predetermined interval a and designed to have such a width as not to be resolved over the wafer. With this structure, checking precision can be reduced. In this structure, the following three respects are set to be conditions and pattern precision is decided for the assist bar. The following is taken into consideration. Only whether the following conditions are satisfied is set to be a checking condition, and a decision of "accepted" is given if the condition is satisfied:

1. Whether each of the assist bars 602a to 602d overlaps with the body pattern 601 through a defect in an enlarging direction (an increase in a pattern);

2. Whether the pattern of the assist bar is resolved over the wafer through the defect in the enlarging direction (the increase in the pattern); and

3. Whether the pattern of the assist bar over the mask disappears through the defect in a reducing direction (a decrease in the pattern).

[0153]

In the embodiment, a classification into two portions is carried out, that is, the body data pattern is set to be a pattern rank PA and the assist bar is set to be a pattern rank PB, and furthermore, the result of the assist bar is decided according to the checking condition determined in accordance with the three specific checking conditions.

Thus, it is possible to form a photomask at a higher speed with a high yield.

[0153]

(Sixteenth Embodiment)

Next, a sixteenth embodiment of the invention will be described.

Description will be given to the check of a mask comprising a phase shift pattern referred to as an enhancer mask for a contact. This technique serves to form a pattern having a high resolution through a main opening portion and a sub-opening portion provided on a periphery thereof in order to implement a very fine process. The main opening portion of the mask inverts the phase of a translucent substrate to be a mask base member by 180 degrees through digging to have the same phase as the phase of a shielding film formed in a halftone surrounding the main opening portion (a difference of 360 degrees).

In the embodiment, as shown in Fig. 22, there are used a body pattern 701 constituting the main opening portion, and four sub-opening portions 702a to 702d separated from the body pattern 701 along the peripheral edge of the body pattern 701

by a predetermined interval d1 and designed to have such a width as not to resolve the opening portion itself over the wafer. With this structure, checking precision can be reduced. In this structure, the following two respects are set to be conditions and pattern precision is decided for the sub-opening portion. The following is taken into consideration. Only whether the following conditions are satisfied is set to be a checking condition, and a decision of "accepted" is given if the condition is satisfied:

1. Whether the sub-opening portion overlaps with each of the body patterns 702a to 702d through a defect in an enlarging direction (an increase in a pattern); and

2. Whether the pattern of the sub-opening portion disappears through the defect in a reducing direction (a decrease in the pattern).

[0153]

In the embodiment, a classification into two portions is carried out, that is, the pattern of the body opening portion is set to be a pattern rank PA and the pattern of the sub-opening portion is set to be a pattern rank PB, and furthermore, the result of the sub-opening portion is decided according to the checking condition determined in accordance with the two specific checking conditions.

Thus, it is possible to form a photomask at a higher speed with a high yield.

[0153]

(Seventeenth Embodiment)

Next, a seventeenth embodiment of the invention will be described below.

While the description has been given to the enhancer mask having the opening portion for a contact constituted by the main opening portion and the sub-opening portion in the embodiment, there will be described the check of a mask comprising a phase shift pattern referred to as an enhancer mask for a line. Referring to the mask, a phase shift of 180 degrees is arranged in a body pattern 801 comprising a shielding portion constituting

a line pattern to form a thin line, and a portion other than the body pattern constitutes an opening of 0 degree.

In the embodiment, as shown in Fig. 23, the body pattern 801 constituting the shielding portion constituted by a halftone pattern is formed and a phase shifter pattern 802 of 180 degrees is formed in the body pattern 801, and the phase shifter pattern itself is designed to have such a width as not to be resolved over the wafer. With this structure, checking precision for the phase shifter pattern can be reduced. In this structure, accordingly, the following two respects are set to be conditions and pattern precision is decided by setting checking precision for the phase shifter pattern to be a rank B and the other checking precision to be a rank A.

The phase shifter pattern is decided as to only whether the following conditions are satisfied. The following is taken into consideration. Only whether the following conditions are satisfied is set to be a checking condition, and a decision of "accepted" is given if the condition is satisfied:

1. Whether the phase shifter pattern 802 overlaps with the body pattern 801 through a defect in an enlarging direction (an increase in a pattern); and

2. Whether the pattern of the phase shifter disappears through the defect in a reducing direction (a decrease in the pattern).

[0153]

In the embodiment, a classification into two portions is carried out, that is, the body pattern is set to be a pattern rank PA and the phase shifter is set to be a pattern rank PB, and furthermore, the result of the phase shifter is decided according to the checking condition determined in accordance with the two specific checking conditions.

Thus, it is possible to form a photomask at a higher speed with a high yield.

[0153]

(Eighteenth Embodiment)

Next, an eighteenth embodiment of the invention will be described.

Description will be given to the check of a mask applied to a super-resolution technique using a chromless phase shift mask referred to as CPL (Chromless Phase Lithography) in a phase shift mask. This technique serves to carry out the formation of a pattern having a high resolution by four phase shifter patterns 902a to 902d comprising a thin pattern which cannot be resolved by itself in place of a body pattern 901 which is resolved to implement a very fine process. The phase shifter pattern of the mask is constituted by a halftone mask.

In the embodiment, as shown in Fig. 24(b), there are used four phase shifter patterns 902a to 902d formed to have the same width in total as that of the body pattern 901 (Fig. 24(a)). With this structure, the checking precision of the phase shifter pattern can be more reduced than that of the body pattern. In this structure, the following three respects are set to be conditions and pattern precision is decided for the phase shifter pattern.

The following is taken into consideration. Only whether the following conditions are satisfied is set to be a checking condition, and a decision of "accepted" is given if the condition is satisfied:

1. Whether the phase shifters overlap with each other through a defect in an enlarging direction (an increase in a pattern);
2. Whether the phase shifter pattern disappears through the defect in a reducing direction (a decrease in the pattern); and
3. A checking sensitivity in a portion corresponding to the edge of the body pattern is not reduced.

[0153]

In the embodiment, a classification into two portions is carried out, that is, the body pattern is set to be a pattern rank PA and the phase shifter pattern is set to be a pattern rank PB, and furthermore, the result of the phase shifter pattern is decided according to the checking condition determined in accordance with the three specific checking conditions.

[0153]

In a phase shift mask using a so-called gate shrink

technique in which a thin gate is formed with an interposition between shifters having different phases, moreover, a mask sensitivity is to be increased in only shifter edges opposed to each other and the checking precision may be decreased in other portions.

[0153]

Thus, it is possible to form a photomask at a higher speed and with a high yield which is suitable for a feature reference.

If a classification in two stages is carried out, that is, the precision rank is once classified depending on whether the pattern has the same node, and is then classified depending on whether the pattern is dummy, consequently, the processing can be carried out at a higher speed and the yield can be enhanced.

[Advantage of the Invention]

[0153]

As described above, according to the photomask checking method in accordance with the invention, all patterns and areas are checked with allowable defect precision of a pattern interval which is conventionally the toughest. However, it is possible to implement the check with necessary precision for each region, each pattern or each edge. As a result, it is not necessary to correct a pattern which is rejected with unnecessary checking precision. Consequently, it is possible to reduce portions to be corrected. Thus, it is possible to reduce a time required for manufacturing the photomask and a manufacturing cost.

[Brief Description of the Drawings]

Fig. 1 is a checking flow chart showing a photomask checking method according to a first embodiment of the invention,

Fig. 2 is a view showing a semiconductor integrated circuit to be checked according to the first embodiment of the invention,

Fig. 3 is an explanatory view showing the transistor portion of the semiconductor integrated circuit,

Fig. 4 is an explanatory view showing the checking method,

Fig. 5 is a flow chart showing a checking step in the checking flow according to the first embodiment of the invention,

Fig. 6 is a view showing a checking method according to

a second embodiment of the invention,

Fig. 7 is a view showing a checking method according to a third embodiment of the invention,

Fig. 8 is a view showing a checking method according to a fourth embodiment of the invention,

Fig. 9 is a view showing a checking method according to a fifth embodiment of the invention,

Fig. 10 is a flow chart showing the checking method according to the fifth embodiment of the invention,

Fig. 11 is a view showing a checking method according to a sixth embodiment of the invention,

Fig. 12 is a view showing a checking method according to a seventh embodiment of the invention,

Fig. 13 is a view showing a checking method according to an eighth embodiment of the invention,

Fig. 14 is a view showing a checking method according to a ninth embodiment of the invention,

Fig. 15 is a diagram showing a checking method according to a tenth embodiment of the invention,

Fig. 16 is a chart showing a checking method according to an eleventh embodiment of the invention,

Fig. 17 is a view showing the checking method according to the eleventh embodiment of the invention,

Fig. 18 is a view showing a checking method according to a twelfth embodiment of the invention,

Fig. 19 is a view showing a checking method according to a thirteenth embodiment of the invention,

Fig. 20 is a flow chart showing a checking method according to a conventional example, and

Fig. 21 is a view showing the checking method according to the conventional example.

[Description of the Reference Numerals and Signs]

1 layout pattern

2 transistor region

3 gate wiring

3T gate wiring on active region

3C region other than gate wiring on active region
4 active region
102 photomask drawing data
103 drawing and process step
104 photomask checking step
105 check accepted product shipment
106 specification of precision from design rule
201 defect of checking precision limitation
202 larger defect than check precision
203 minimum wiring interval
204 wiring interval (which is larger than minimum interval)
210 to 213 pattern arranged with minimum interval
214 to 216 pattern arranged with great width
306 checking precision data

[Designation of Document] Abstract

[Abstract]

[Problem] It is an object to provide a photomask checking method capable of shortening a TAT and reducing a cost.

[Means for Resolution] A method of checking a photomask for a semiconductor integrated circuit formed based on drawing pattern data, includes the steps of classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference and extracting the same, determining checking precision for each of the ranks, and deciding quality of the photomask depending on whether the determined checking precision is satisfied.

[Selected Drawing] Fig. 4

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FIG. 1

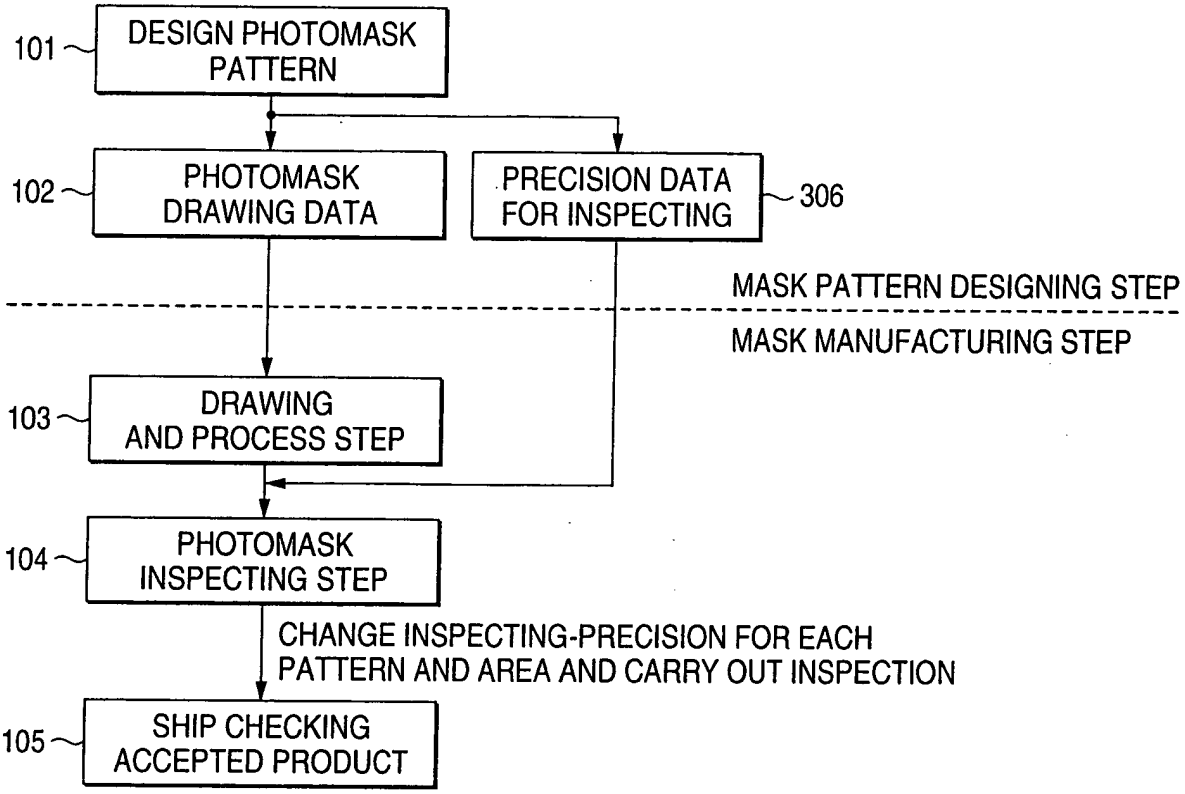


FIG. 2

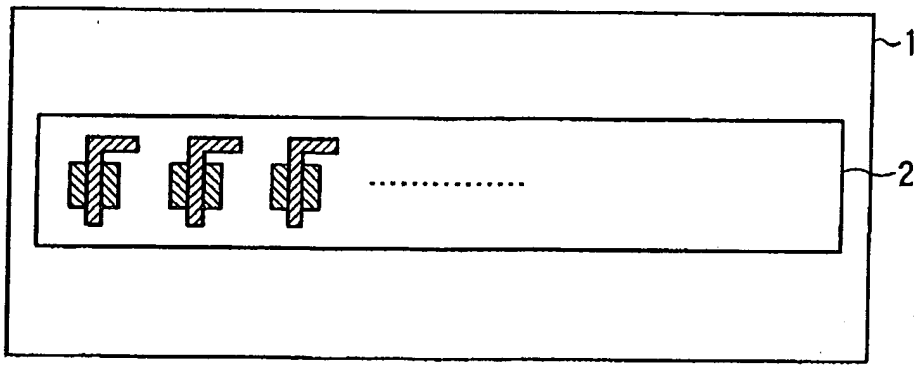


FIG. 3

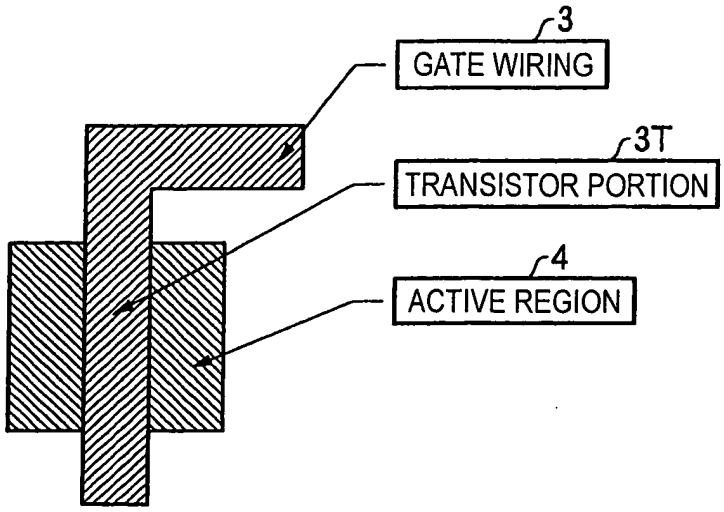

3
GATE WIRING
3T
TRANSISTOR PORTION
4
ACTIVE REGION

FIG. 4

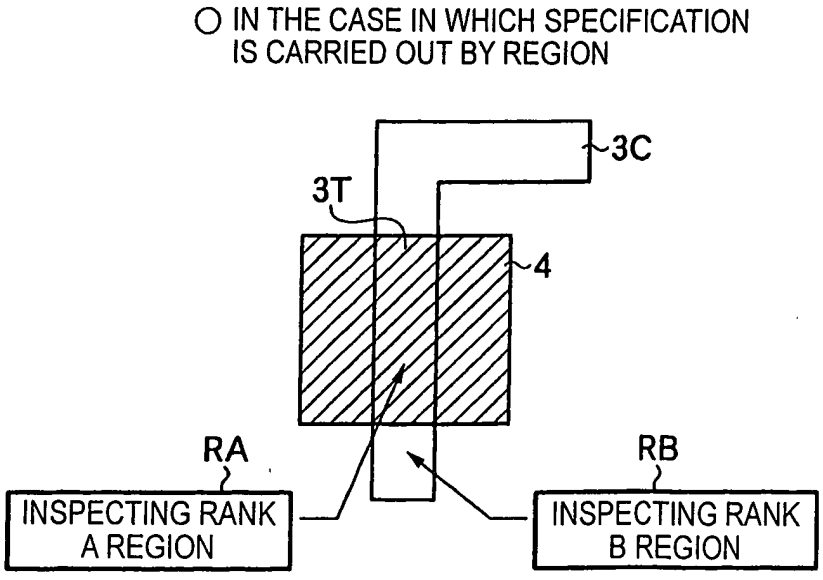

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY REGION
3C
3T
4
RA
INSPECTING RANK A REGION
RB
INSPECTING RANK B REGION

FIG. 5

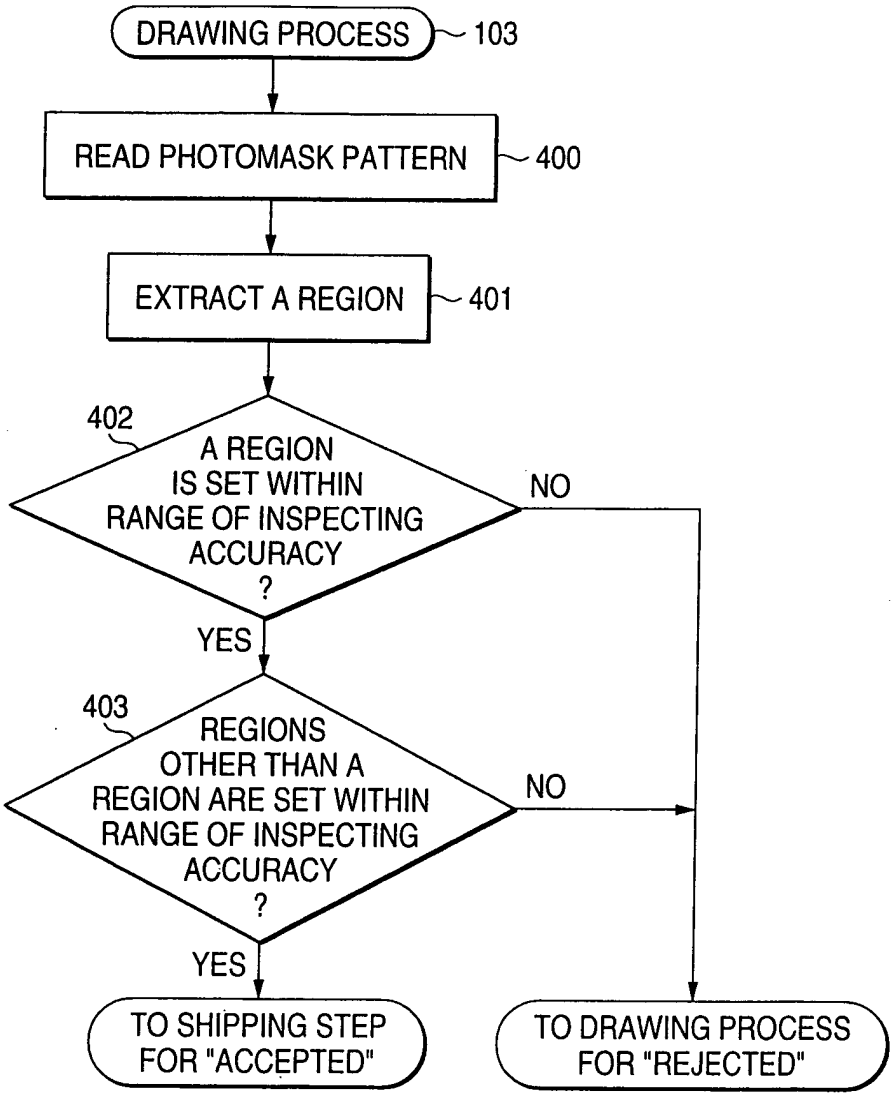

DRAWING PROCESS
103
READ PHOTOMASK PATTERN
400
EXTRACT A REGION
401
402
A REGION IS SET WITHIN RANGE OF INSPECTING ACCURACY ?
NO
YES
403
REGIONS OTHER THAN A REGION ARE SET WITHIN RANGE OF INSPECTING ACCURACY ?
NO
YES
TO SHIPPING STEP FOR "ACCEPTED"
TO DRAWING PROCESS FOR "REJECTED"

FIG. 6

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY PATTERN

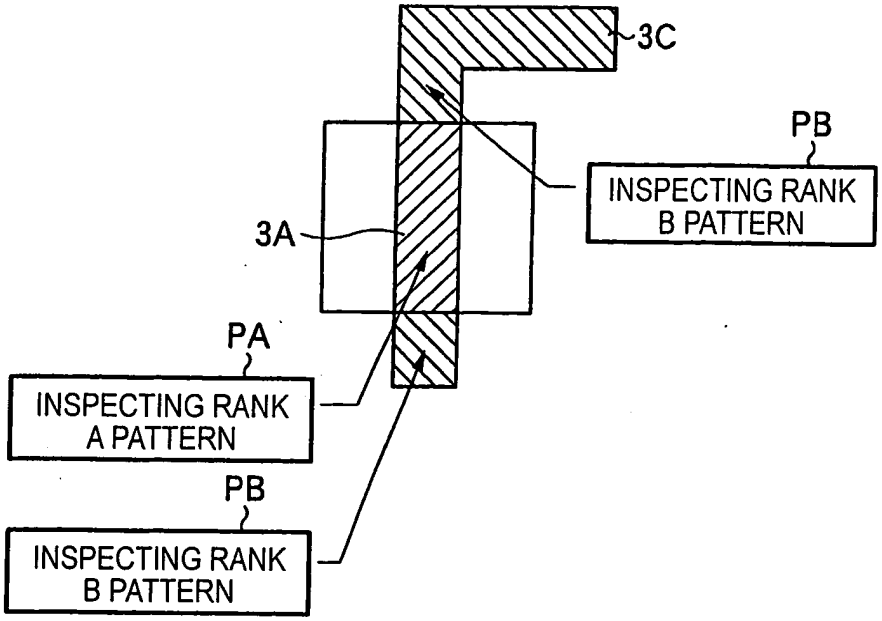


FIG. 7

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY EDGE

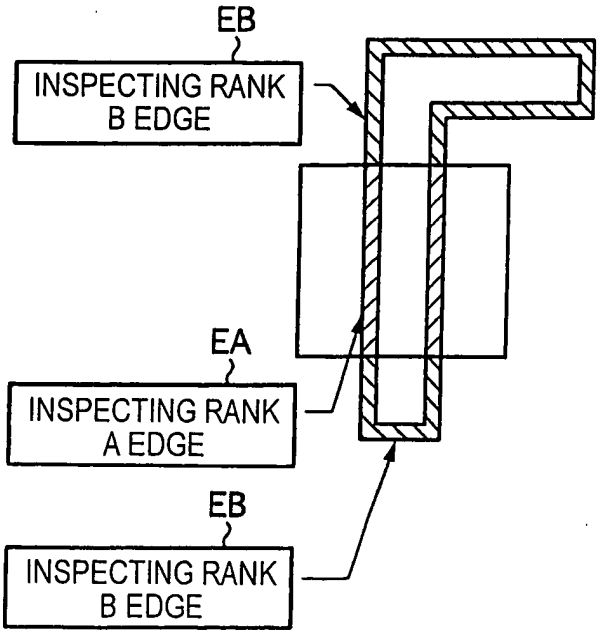


FIG. 8A

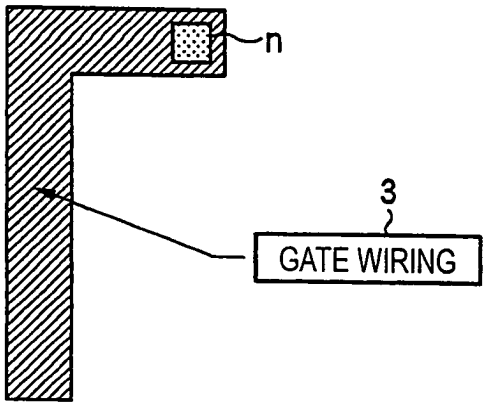


FIG. 8B

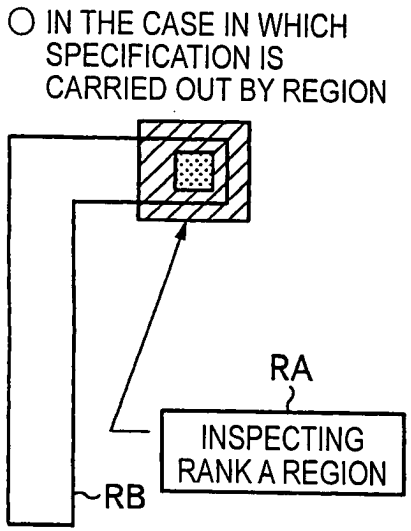


FIG. 8C

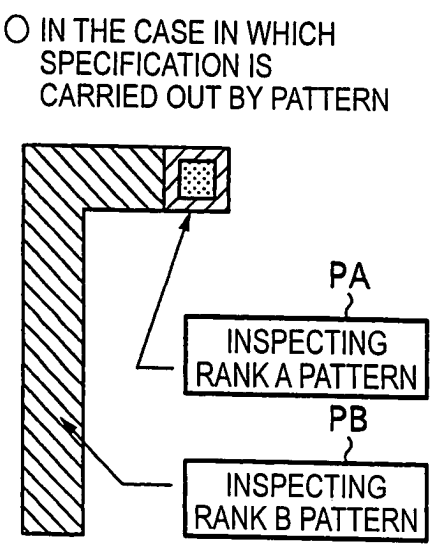


FIG. 8D

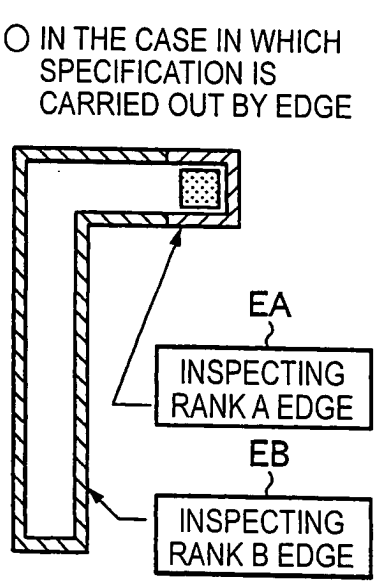


FIG. 9A

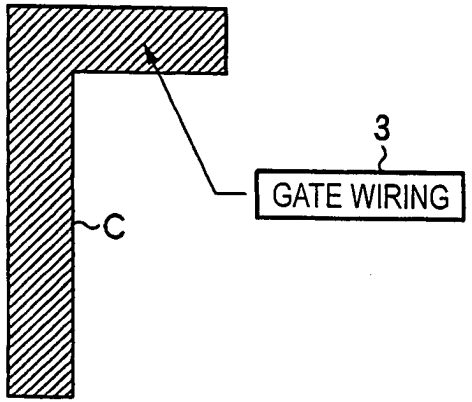


FIG. 9B

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY REGION

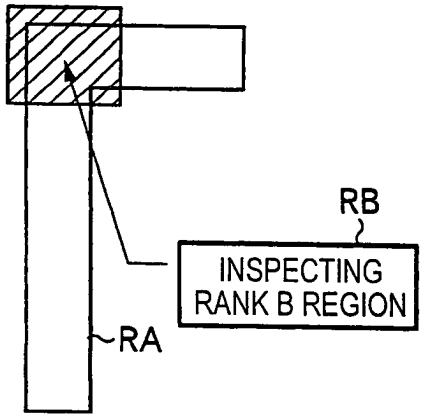


FIG. 9C

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY PATTERN

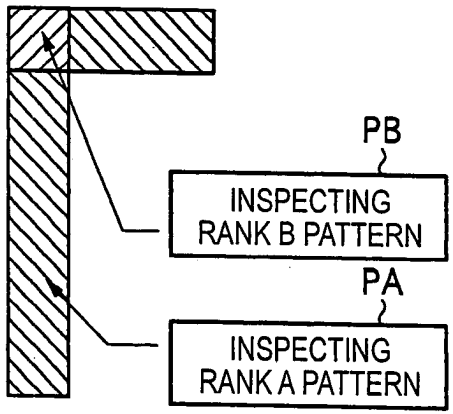


FIG. 9D

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY EDGE

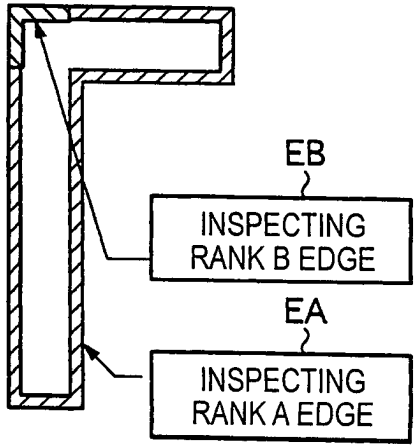


FIG. 10

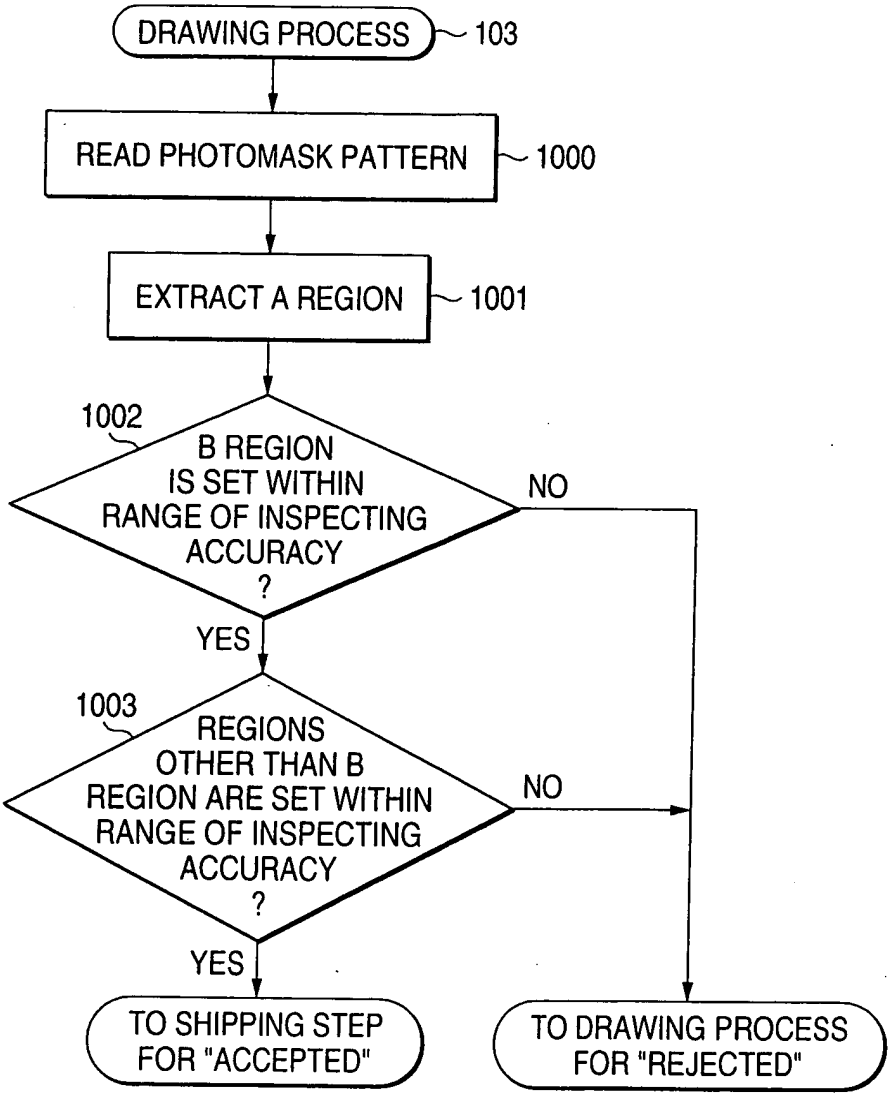

DRAWING PROCESS
103
READ PHOTOMASK PATTERN
1000
EXTRACT A REGION
1001
1002
B REGION IS SET WITHIN RANGE OF INSPECTING ACCURACY ?
NO
YES
1003
REGIONS OTHER THAN B REGION ARE SET WITHIN RANGE OF INSPECTING ACCURACY ?
NO
YES
TO SHIPPING STEP FOR "ACCEPTED"
TO DRAWING PROCESS FOR "REJECTED"

FIG. 11A

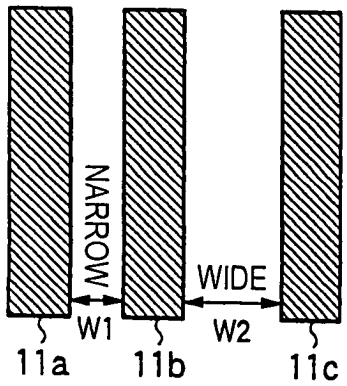


FIG. 11B

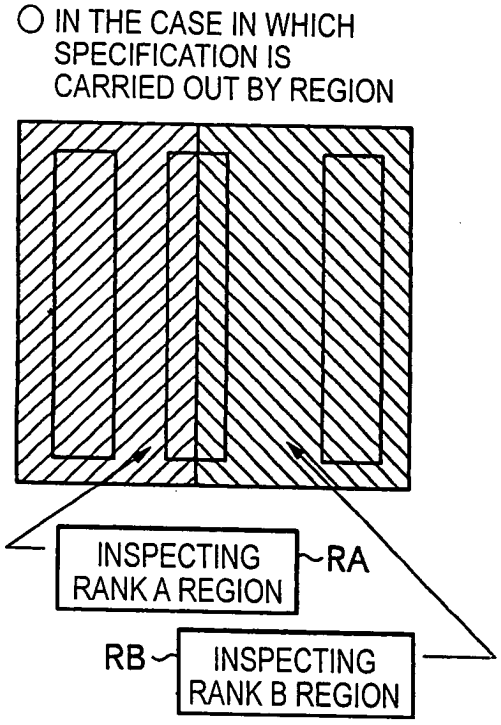


FIG. 11C

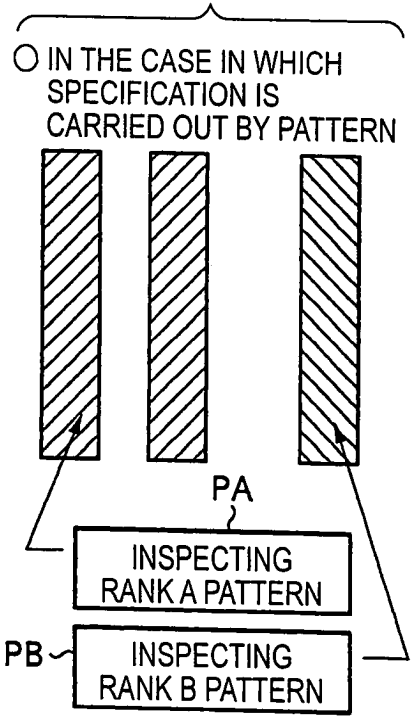


FIG. 11D

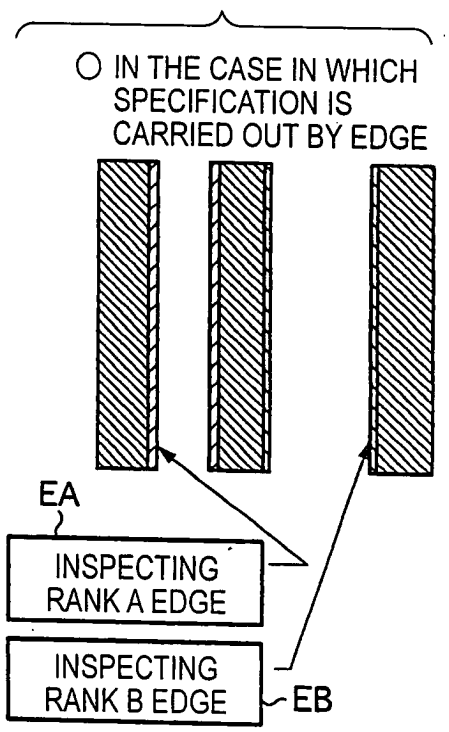


FIG. 12A

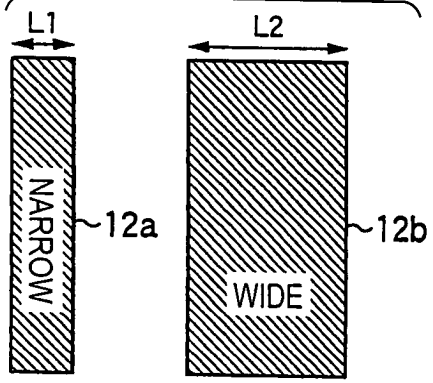


FIG. 12B

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY REGION

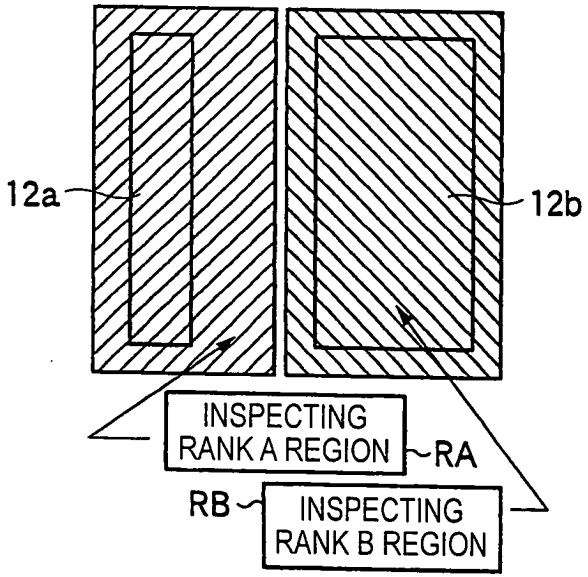


FIG. 12C

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY PATTERN

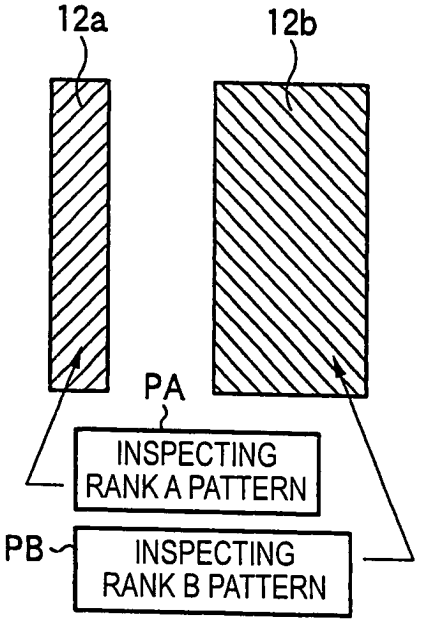


FIG. 12D

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY EDGE

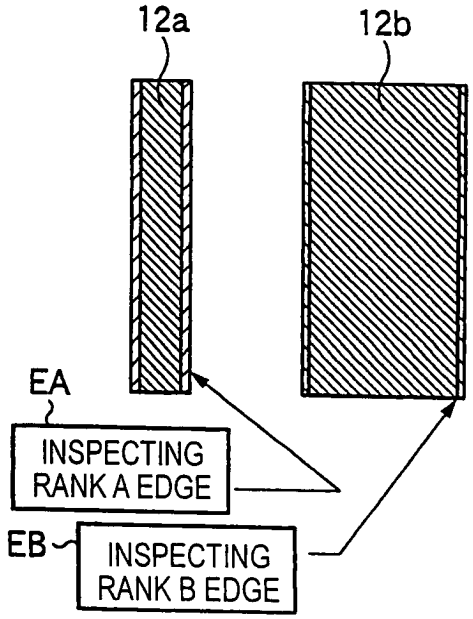


FIG. 13A

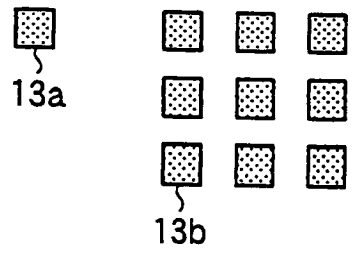


FIG. 13B

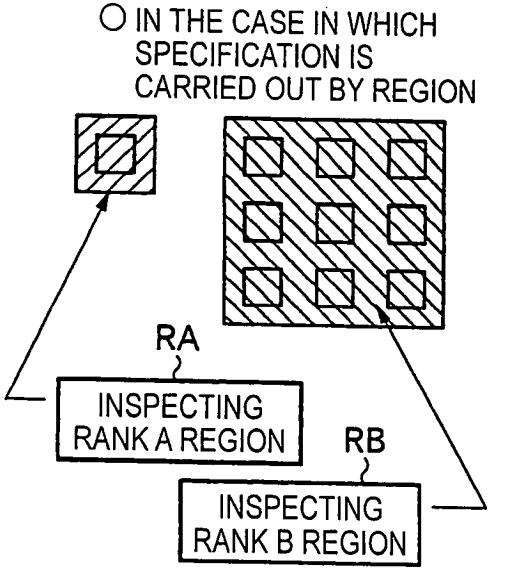


FIG. 13C

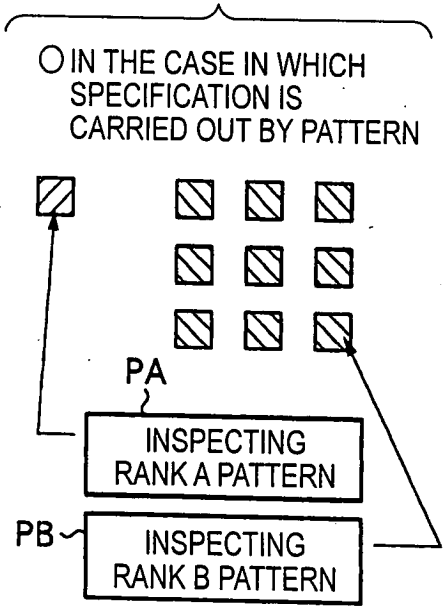


FIG. 13D

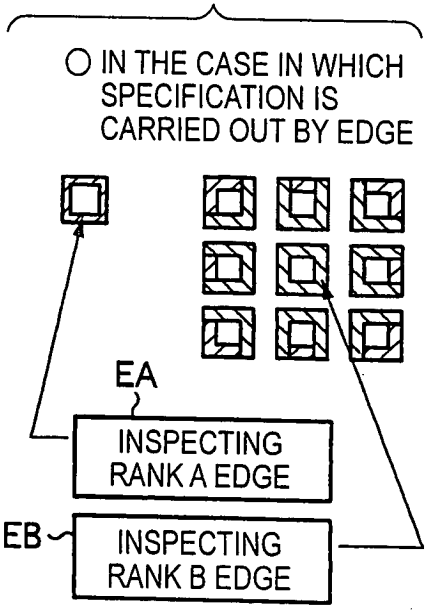


FIG. 14A

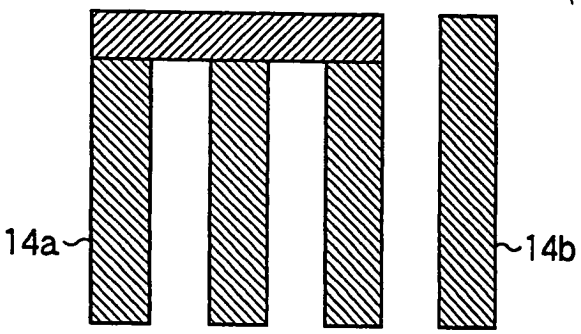


FIG. 14B

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY REGION

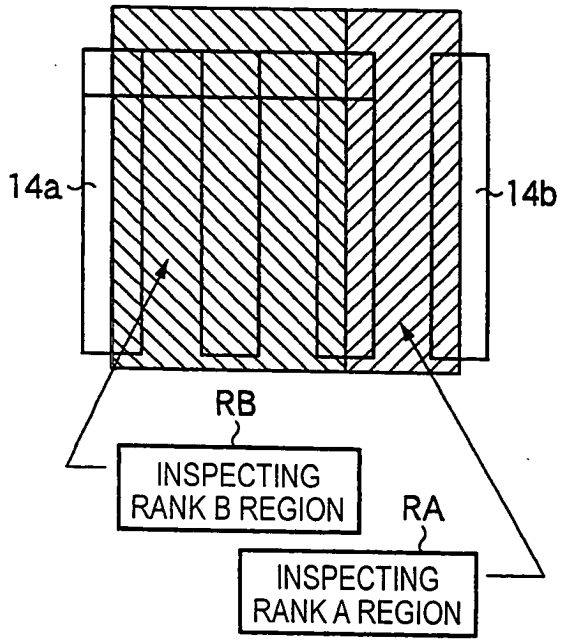


FIG. 14C

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY PATTERN

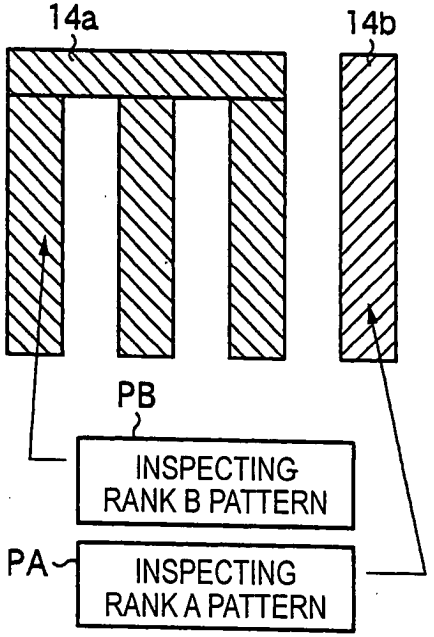


FIG. 14D

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY EDGE

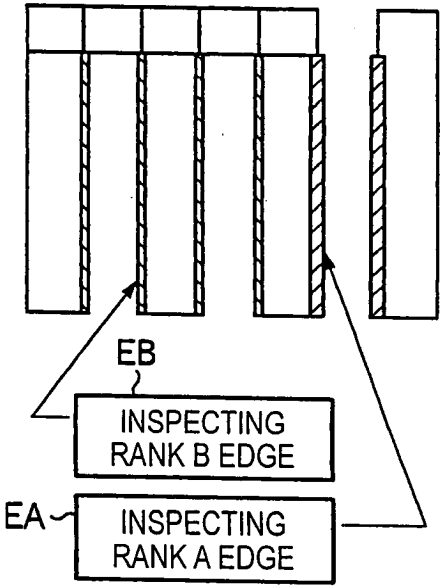


FIG. 15

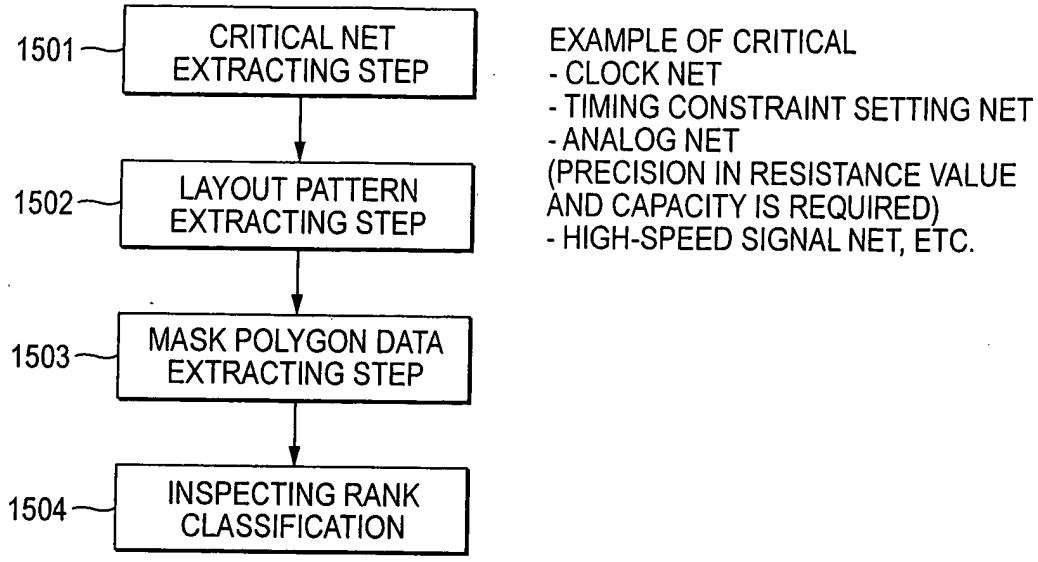

1501
CRITICAL NET EXTRACTING STEP
1502
LAYOUT PATTERN EXTRACTING STEP
1503
MASK POLYGON DATA EXTRACTING STEP
1504
INSPECTING RANK CLASSIFICATION
EXAMPLE OF CRITICAL
- CLOCK NET
- TIMING CONSTRAINT SETTING NET
- ANALOG NET
(PRECISION IN RESISTANCE VALUE AND CAPACITY IS REQUIRED)
- HIGH-SPEED SIGNAL NET, ETC.

FIG. 16

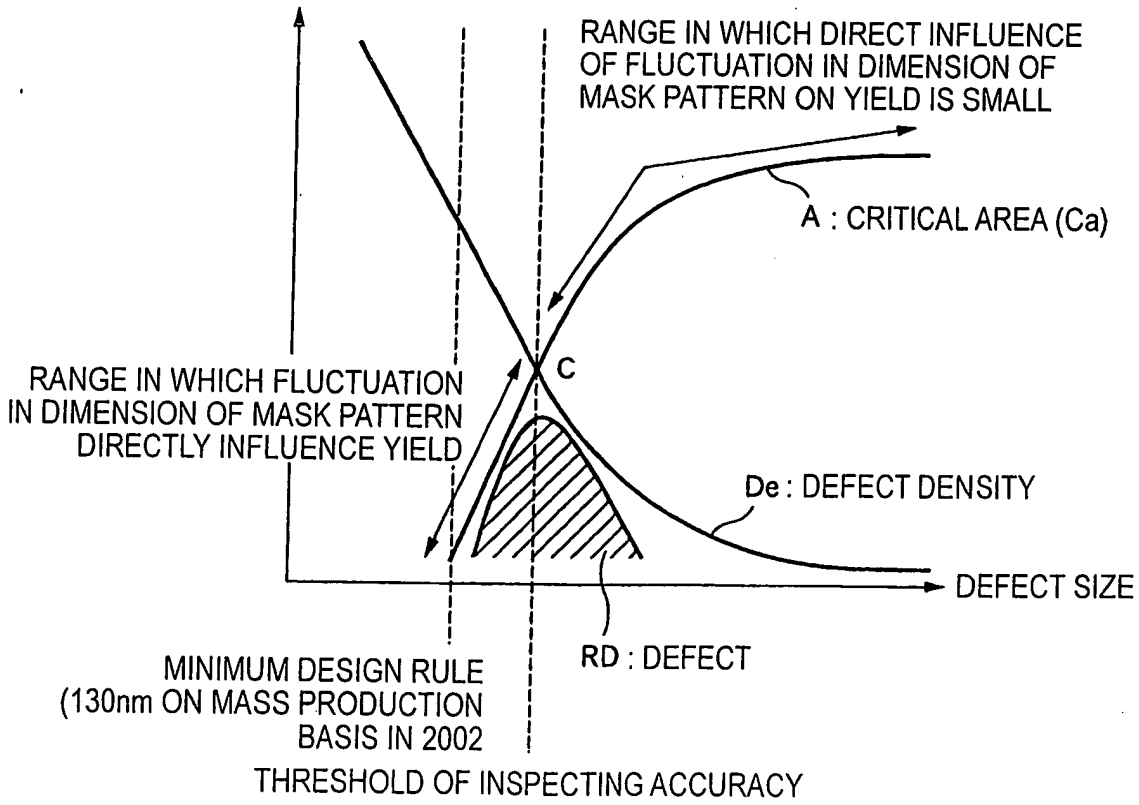
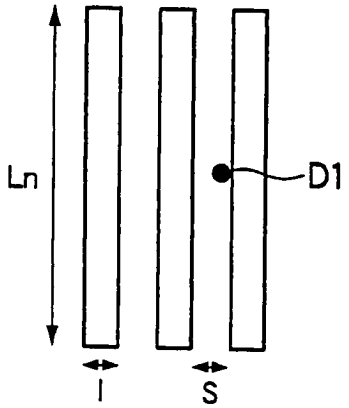

RANGE IN WHICH DIRECT INFLUENCE OF FLUCTUATION IN DIMENSION OF MASK PATTERN ON YIELD IS SMALL
A : CRITICAL AREA (Ca)
C
RANGE IN WHICH FLUCTUATION IN DIMENSION OF MASK PATTERN DIRECTLY INFLUENCE YIELD
De : DEFECT DENSITY
DEFECT SIZE
RD : DEFECT
MINIMUM DESIGN RULE (130nm ON MASS PRODUCTION BASIS IN 2002
THRESHOLD OF INSPECTING ACCURACY

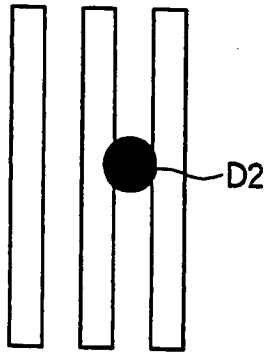
FIG. 17A

SHORT DEFECT AREA = Ln (l+S)



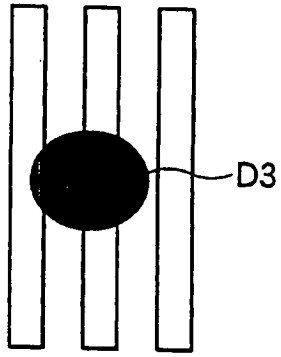
DEFECT SIZE (x) < S
NO SHORT DEFECT
Ca (x) = 0

FIG. 17B



S < DEFECT SIZE (x) < 2l+S
SHORT DEFECT IN SOME PLACES
Ca (x) = Ln (l+S)(X-S)/(l+S)

FIG. 17C



2l+S < DEFECT SIZE (x)
SHORT DEFECT IN ALL PLACES
Ca (x) = Ln (l+S)

FIG. 18A

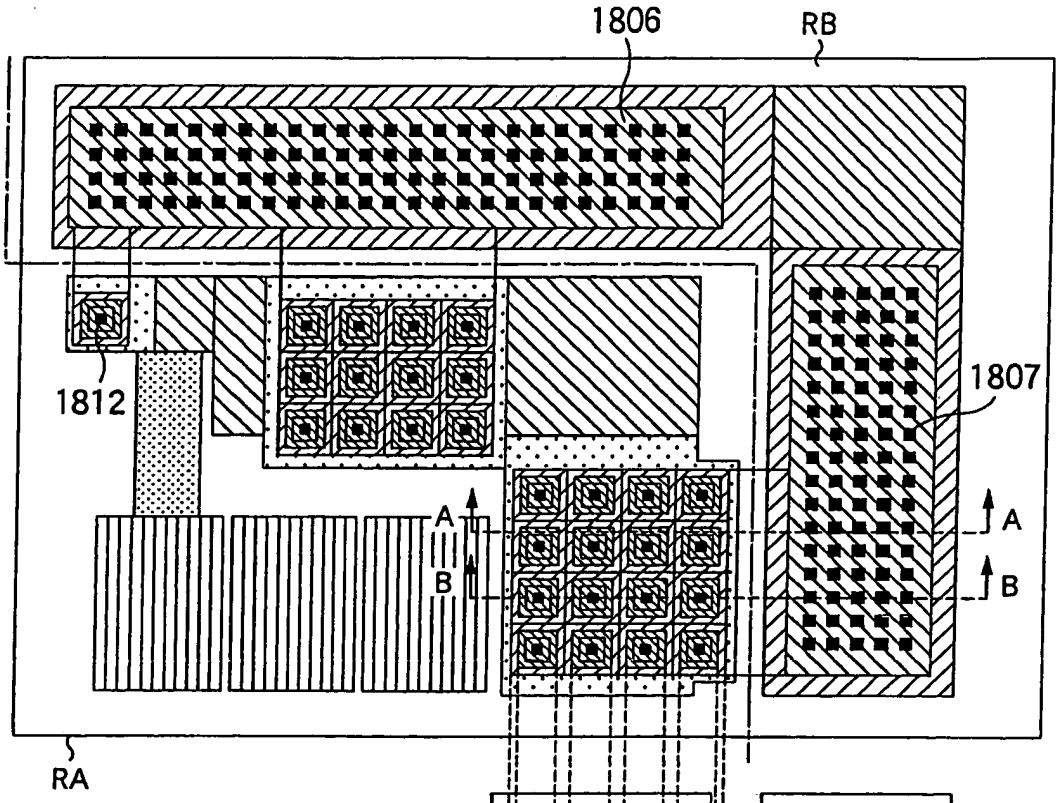


FIG. 18B A-A

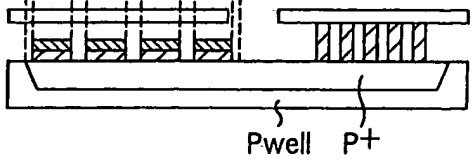
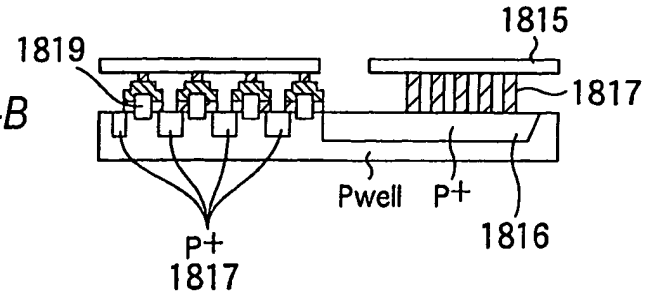


FIG. 18C B-B



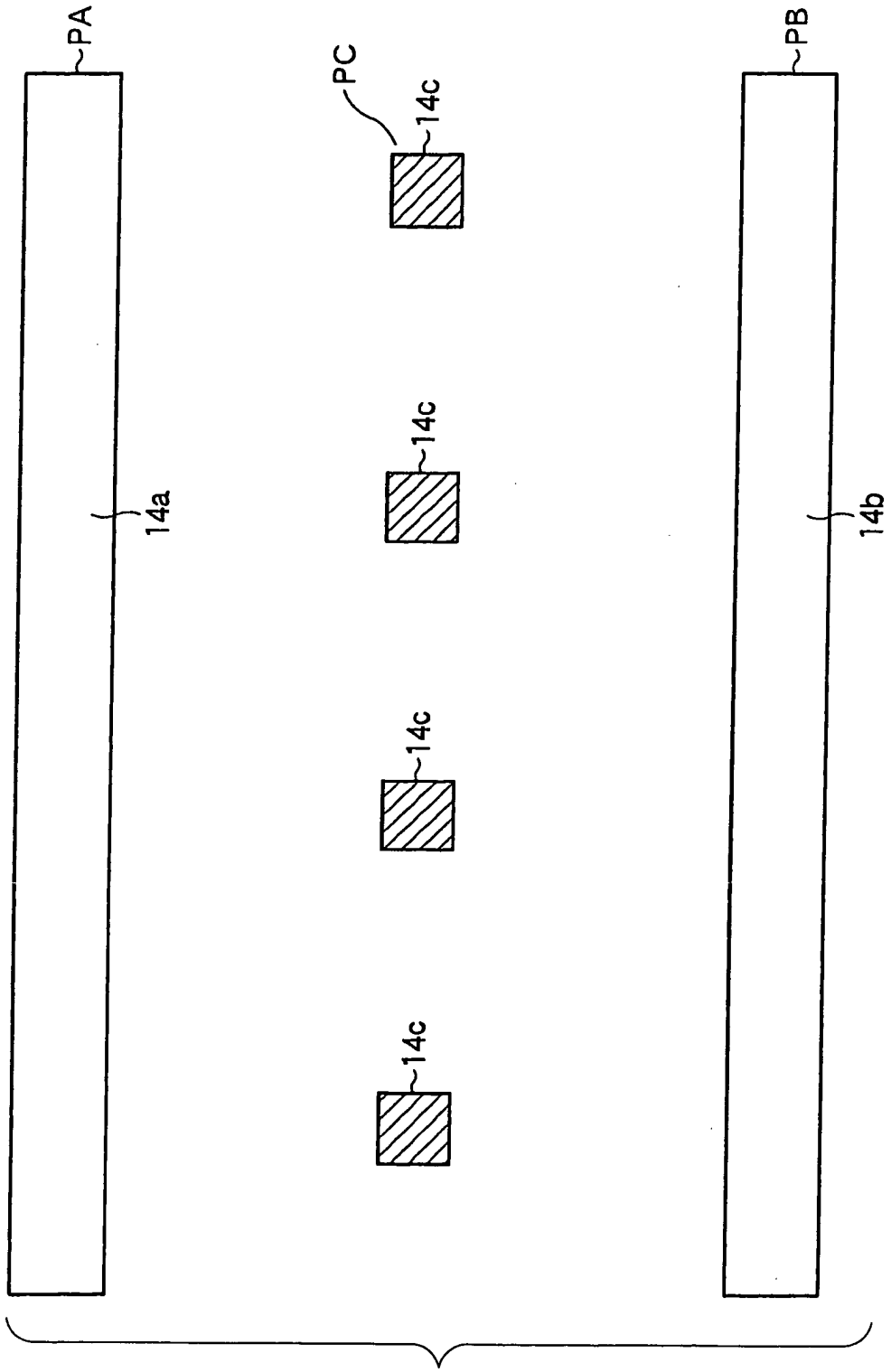


FIG. 19

FIG. 20

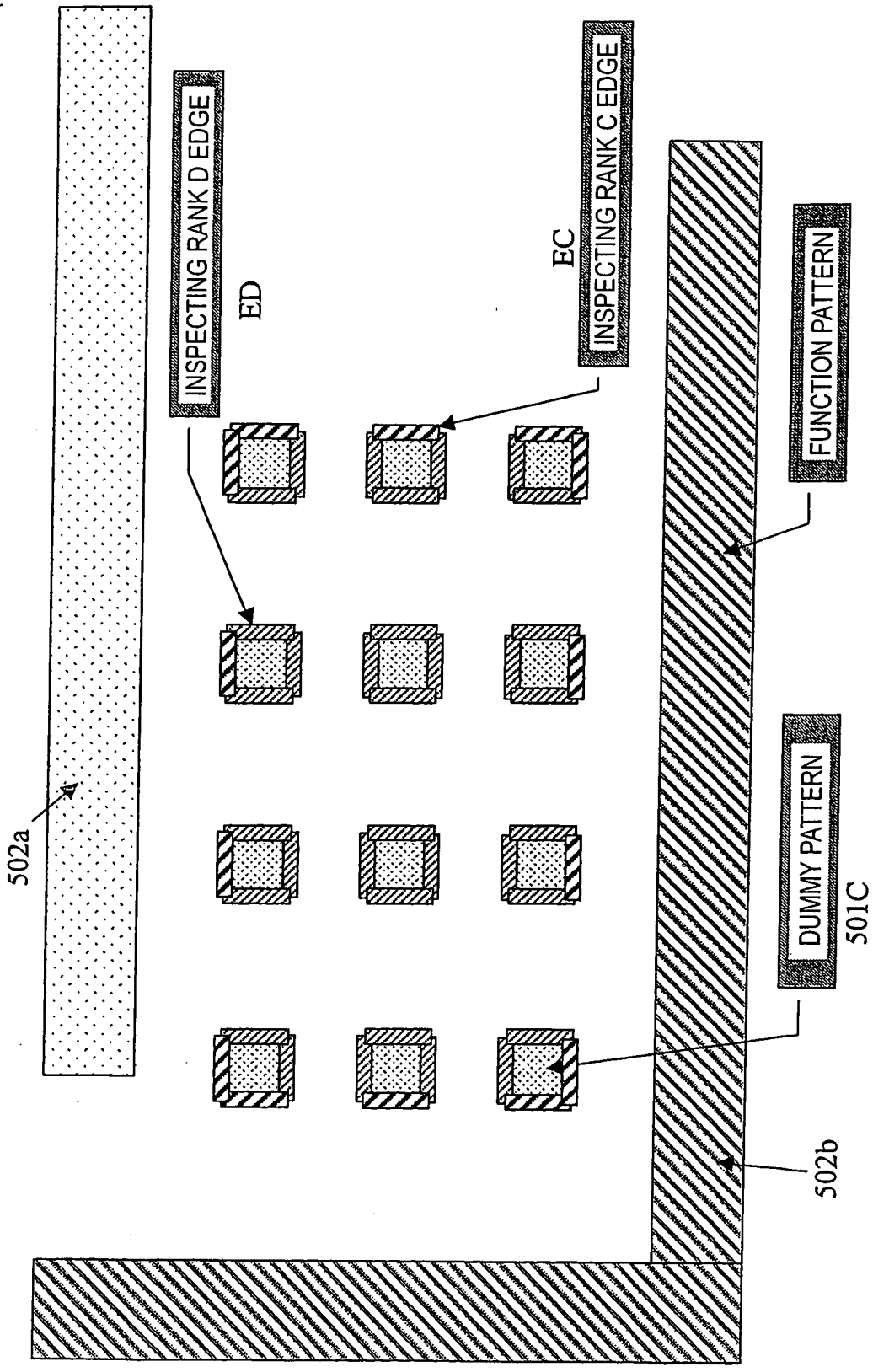

INSPECTING RANK D EDGE
ED
EC
INSPECTING RANK C EDGE
FUNCTION PATTERN
502a
DUMMY PATTERN
501C
502b

FIG. 21

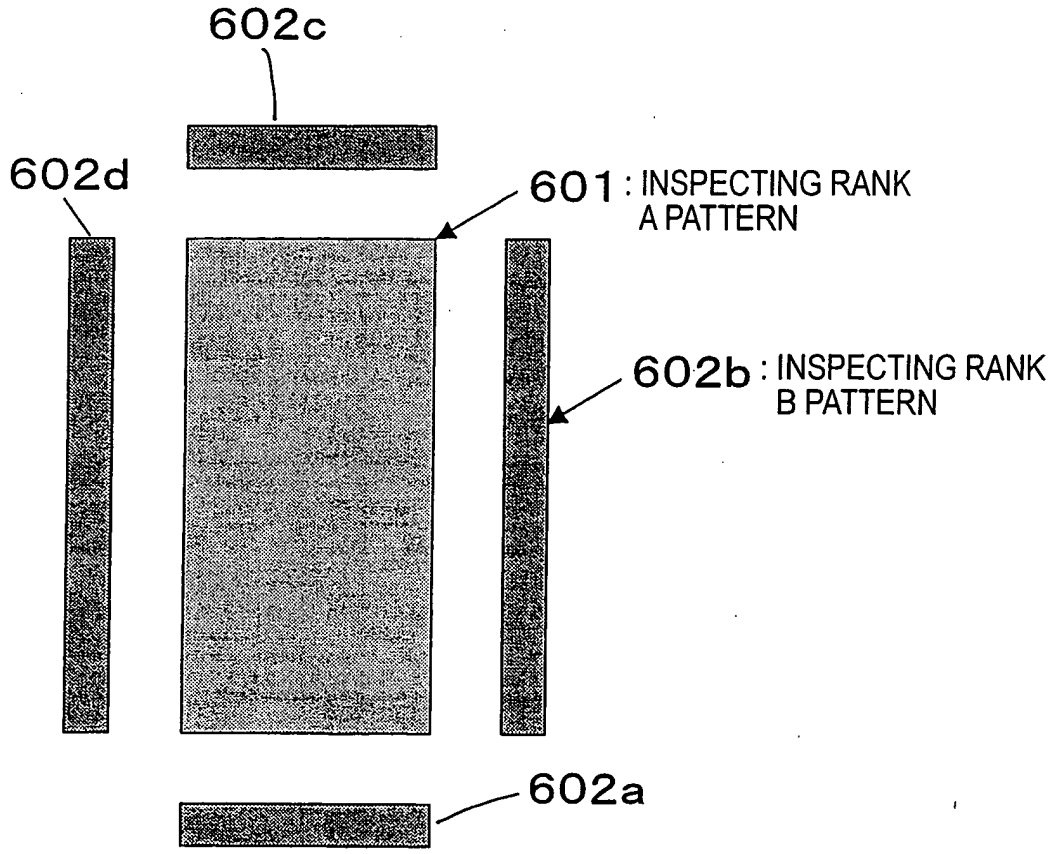

602c
602d
601 : INSPECTING RANK A PATTERN
602b : INSPECTING RANK B PATTERN
602a

FIG. 22

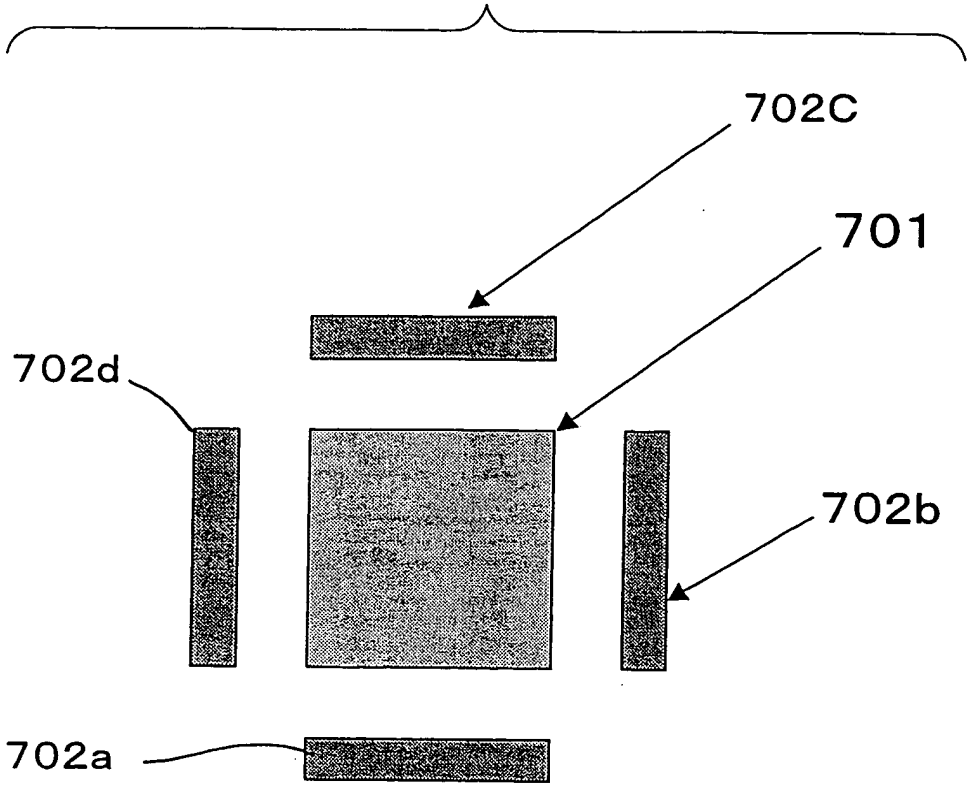


FIG. 23

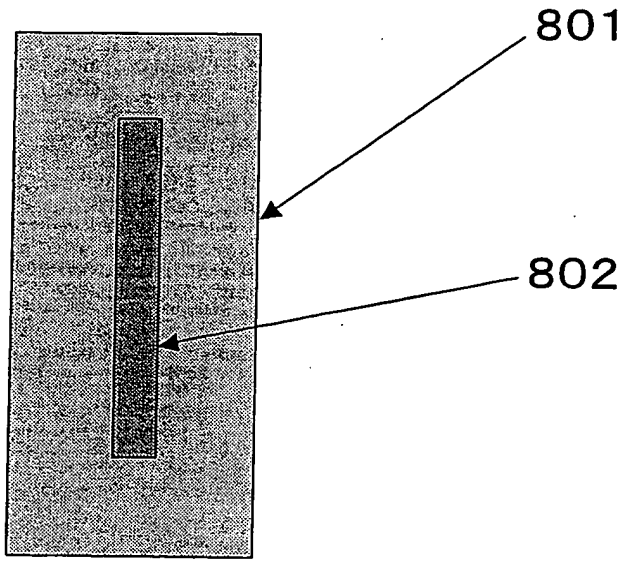


FIG. 24B

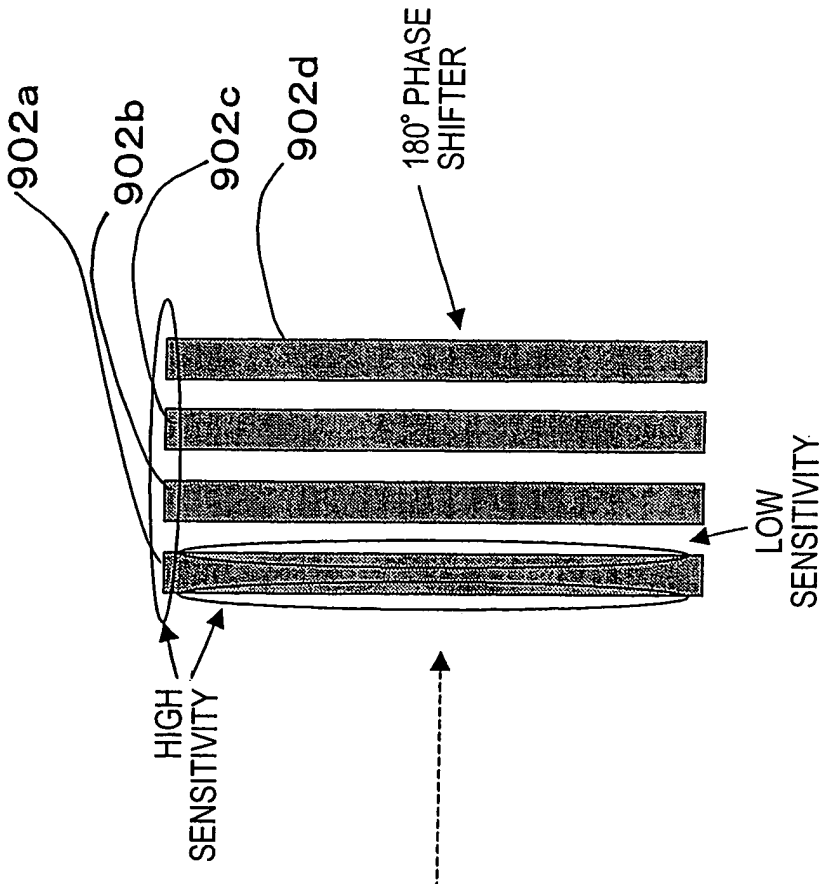


FIG. 24A

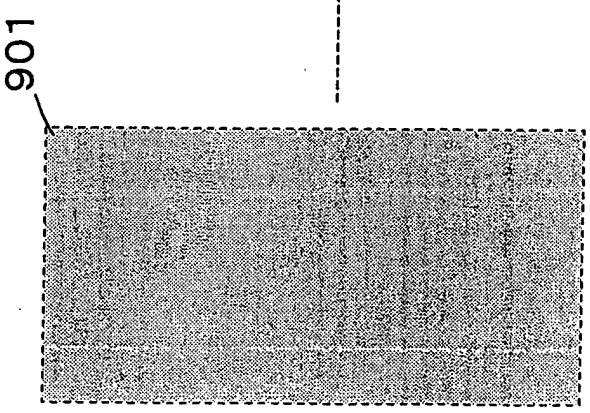


FIG. 25

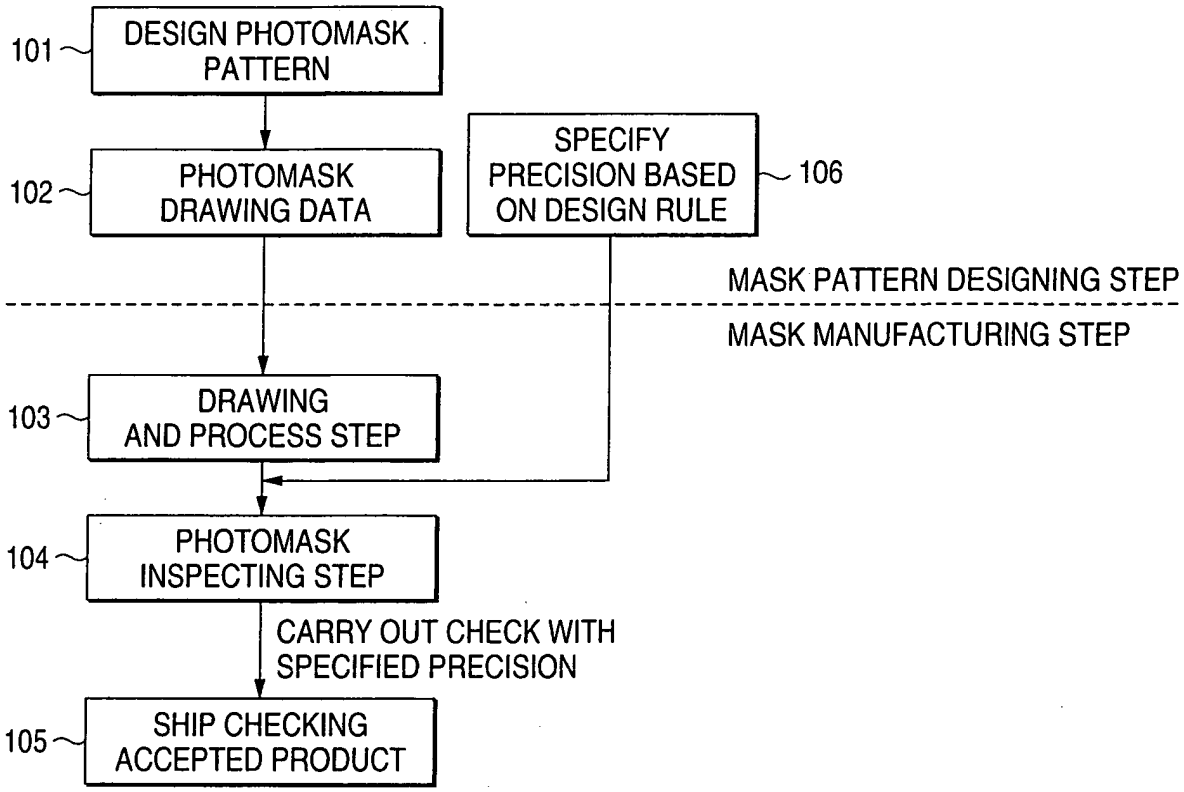

101
DESIGN PHOTOMASK PATTERN
102
PHOTOMASK DRAWING DATA
SPECIFY PRECISION BASED ON DESIGN RULE
106
MASK PATTERN DESIGNING STEP
MASK MANUFACTURING STEP
103
DRAWING AND PROCESS STEP
104
PHOTOMASK INSPECTING STEP
CARRY OUT CHECK WITH SPECIFIED PRECISION
105
SHIP CHECKING ACCEPTED PRODUCT

FIG. 26B

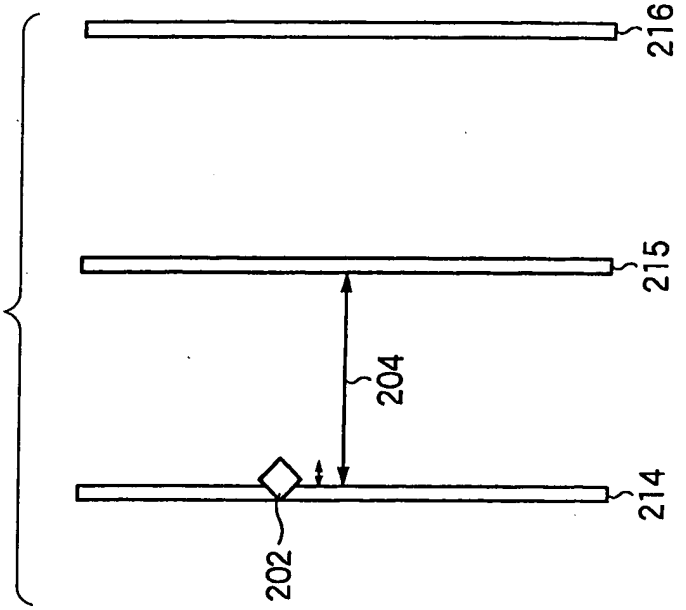
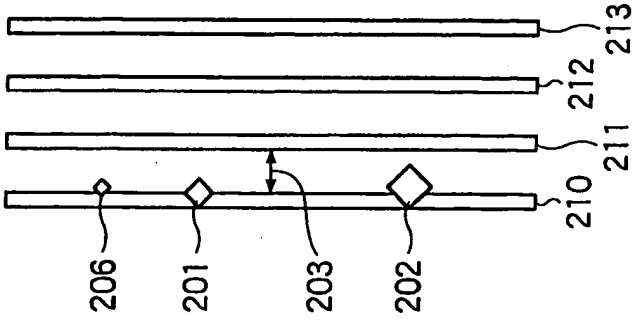


FIG. 26A



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